# Study of Single Event Effects on 28nm ARM Core Testing Chip

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By

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# ABSTRACT

With the development of silicon technologies, the minimum feature size of transistors has scaled down to several nanometers. This remarkably increases the number of transistors on a single chip, leads to improved circuit performance and reduced cost. However, Single Event Effects (SEE) induced by energetic particles are more significant for nanometer CMOS technologies due to the reduction in critical charge, higher clock speeds, lower operating voltages and high circuit densities. Research studies have shown that, compared to bulk technologies, silicon on insulator (SOI) technologies reduces the charge collection length of incident ions leading to less collected charge, and thus lower SEE sensitivity. STMicroelectronics' 28-nm fully depleted SOI technology has shown superior performance in terms of single event effects resistance, compared to those of 28-nm bulk technologies. The reduced SEE sensitivity as well as the Single Event Latch-up immunity makes this technology attractive for harsh radiation environments such as space. Previous work has focused on devices or small circuits, however, the overall SEE performance in complex circuits at different operating conditions needs to be further investigated. Microprocessors are widely used in avionics and space applications due to their performance and extensive tool support. It is thus interesting to assess the SEE performance of ARM Cortex-M0 microcontroller cores implemented in the 28-nm FDSOI technology.

In this thesis, the goal is to study signal event effects in a test chip that includes several ARM Cortex-M0 cores designed with different SEE-tolerant levels. The test chip has a triple-module-redundant (TMR) SRAM and an on-chip clock system, which are shared by the ARM cores. The test chip also includes custom-designed SEE-hardened flip-flops and regular flip-flops from the standard cell library, which were connected into two shift-register chains to independently evaluate

their SEE performance. A FPGA-based testing system was developed to test the flip-flop chains and ARM cores. The system includes a raspberry Pi board, a daughter card for the test chip, and the FPGA mother board. Eight different microprocessor testing programs were also developed for the ARM cores. Heavy ion experiments were performed with the testing system. Results showed that the hardened flip-flops have excellent performance, which do not have errors up to 42 $MeV \times cm^2/mg$ of LET. The SRAM were also tested separately during heavy ion experiments and it showed that the SRAMs without TMR protection are sensitive to SEEs, however, the TMR can effectively protect the SRAM from SEEs. Two ARM Cortex-M0 cores were also evaluated with the heavy ion experiments. The results showed that the ARM core with hardened flip-flops has improved performance compared to the reference core which was implemented with regular cells from the standard library. To the author's knowledge, this is the first published work where two different implementations of the same processor core have been evaluated under heavy ion irradiation.

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# List of Abbreviations

| | |
|---|---|
| AHB | Advanced High-performance Bus |
| AMBA | Advanced Microcontroller Bus Architecture |
| ARM | Advance RISC Machine |
| CMOS | Complementary Metal Oxide Semiconductor |
| CRC | Cyclic Redunancy Check |
| DCM | Digital Clock Manager |
| DFF | D Flip-flop |
| DICE | Dual Interlocked Storage Cell |
| DRAM | Dynamic Random-Access Memory |
| DUT | Device under Test |
| FDSOI | Fully Depleted Silicon On Insulator |
| FF | Flip-flop |
| FFT | Fast Fourier Transform |
| FIT | Failure in Time |
| FPGA | Feild Programmable Gate Array |
| FSM | Finite State Machine |
| HISEEIF | Heavy Ion Single Event Irradiation Facility |
| I2C | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| LBNL | Lawrence Berkeley National Lab |
| LET | Liner Energy Transfer |
| LOF | List of Figures |
| LOT | List of Tables |
| MCU | Multiple Cells Upset |
| MOS | Metal Oxide Semiconductor |
| MUX | Multiplexer |
| NMOS | Negative-channel Metal Oxide Semiconductor |

| | |
|---|---|
| NSREC | Nuclear and Space Effects Conference |
| PDSOI | Partially Depleted Silicon On Insulator |
| PMOS | Positive-channel Metal Oxide Semiconductor |
| RISC | Reduced Instruction Set Computing |
| RO | ring oscillator |
| SBU | Single Bit Upset |
| SCUBA | Self Contained Underwater Breathing Apparatus |
| SEE | Single Event Effect |
| SEL | Single Event Latchup |
| SER | Soft Error Rate |
| SET | Single Event Transient |
| SEU | Single Event Upset |
| SOI | Silicon On Insulator |
| SPA | Single-Photon Absorption Lasers |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random Access Memories |
| SSSA | Saskatchewan Structural Sciences Centre |
| TMR | Triple Module Redundancy |
| TPA | Two-Photon Absorption Lasers |
| UART | universal asynchronous receiver-transmitter |
| NRL | U.S. Naval Research Laboratory |

# 1 INTRODUCTION

## 1.1 Background

When energetic particles strike integrated circuits (ICs), they may cause unexpected errors, which are called Single Event Effects (SEEs). These energetic particles can come from space or the decay of radioactive atoms from semiconductor materials [6].

After Binder et al., first reported and investigated unexpected errors in satellite circuit components caused by cosmic rays in 1975 [7], other SEEs were discovered from unexplained resource. Four years later, two Intel's engineers, May and Woods, discovered that alpha particles can also produce single-bit errors in terrestrial memory circuits [8]. In their study, they also defined the term of "soft error," which is an error that is random, non-permanent, and recoverable. This phenomenon, that the data in memory circuits had flipped, was also reported by IBM, from data accumulated and analyzed from 1978 to 1994 [6], and illustrated that a SEE could be caused by space rays or spontaneous fission in a terrestrial environment. Single Event Upsets (SEUs) as the main source of soft errors have attracted attention from increasing numbers of scientists and engineers, and several papers were published in the IEEE Nuclear and Space Effects Conference (NSREC) in the late 1970s [9, 10]. As the name implies, an SEU occurs when a single radiation particle strikes a memory cell, such as a flip-flop or register, and generates electron-hole pairs which leads to an upset or reverses the logic state in a sequential circuit unit. Like SEUs, if a single event occurs in

a combinational logic and the transient propagates into a following register or memory element, it is referred to as a Single Event Transient (SET). Both of SEUs and SETs are categorized as SEEs and are referred to as "soft errors" because they do not result in permanent damages to the circuit. These errors can be reversed by rewriting the previous data to replace the erroneous data.

In contrast to "soft errors" caused by SEUs or SETs, single-event latchups (SELs), first reported in 1979 [11], can trigger a parasitic structure, which shorts the power and ground, and potentially leads to permanent destruction in the circuits. The phenomenon of SELs generates crucial reliability concerns for space equipment.

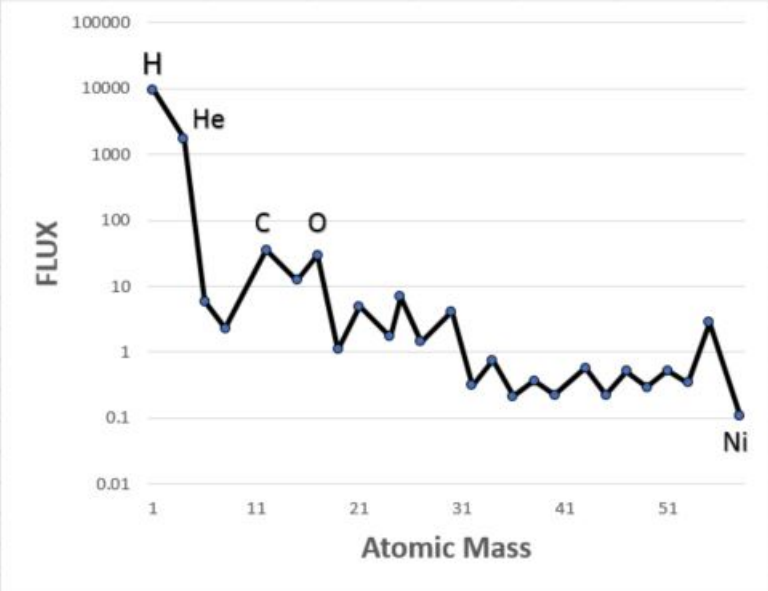



**Figure 1.1:** Particle flux of a cosmic ray [1]

A variety of particles in natural circumstances, such as protons, alpha particles, heavy ions, and neutrons, can lead to SEEs. Protons are one of the major radiation particles in galactic cosmic rays (ie., from outside the solar system) and solar particles, which composing 85% of cosmic rays and 90 to 95% of solar particles, respectively [1]. A proton is a subatomic particle carrying a positive electric charge. As shown in Figure 1.1, in cosmic rays the proton flux is approximately more than

one order of magnitude higher than the helium flux (alpha particles), and is at least two orders of magnitude higher than the flux of carbon, oxygen, or others heavy ions (less than 1%).

Although the protons make up most galactic rays and solar particles, the impact of protons is not more significant than alpha particles or heavy ions in radiation effects. Alpha protons consist of two protons and two neutrons, accounting for 14% of space rays, as Figure 1.1 illustrates. However previous experiments have indicated that alpha particles from packaging materials contribute over 90% of soft errors in Dynamic Random-Access Memory (DRAM) devices in terrestrial environments [12]. Even if heavy ions contribute less than 1% of cosmic rays, they can deposit more energy per unit depth than protons when they penetrate silicon devices and can induce a larger impact on the devices [1]. In some special events in the vicinity of Earth, such as a large solar flare, the proportion of heavy ions can rise to approximate 50% of universe background, while the number of alpha particles and protons in space can increase by thousands of times.

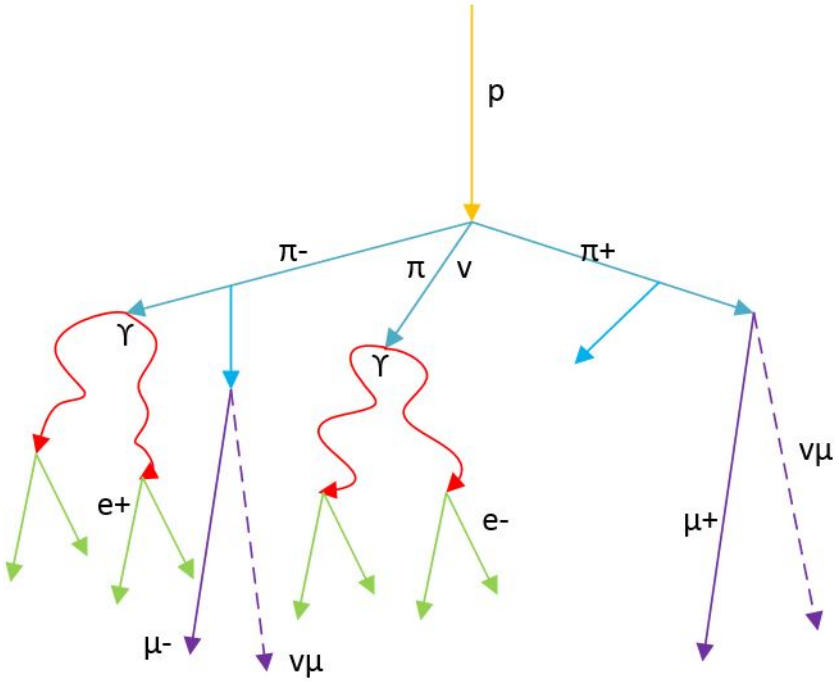



**Figure 1.2:** Flow of an air shower [2]

In contrast to charged particles, such as protons, alpha particles, or heavy ions, neutrons carrying no charge can also cause soft errors through indirect ionization [4]. Furthermore, recent research implies that neutrons are the main cause of SEEs in terrestrial applications [13]. Unlike energetic, charged particles that directly produce a charge in semiconductor materials, neutrons can generate secondary charged particles via nuclear reactions when penetrating integrated circuits (ICs). When cosmic rays penetrate through the atmosphere, it is difficult for them to hit the ground directly, but they will interact with molecules in the air [2]. During the collisions with molecules, the primary particle will produce some second any particles, as shown in Figure 1.2. Neutral pions generated by collisions will decay very rapidly into two gamma rays, but charged pions will remain for a long time before they decay.

Over the past few decades, with the scaling of IC technology, transistor feature size has shrunk, power consumption has decreased, and clock frequency has been enhanced. As a result, ICs have become increasing by complex, and more and more vulnerable to SEEs. Although the Soft Error Rate (SER) per bit is decreasing as the technologies improve, the multiple-cell upset (MCU) rates have significantly increased, and have already exceeded the effects of single bit upsets (SBUs) in Static Random Access Memories (SRAMs) [3]. Figure 1.3 demonstrates the percentage of SBUs and MCUs in different technology nodes in SRAMs.

In order to protect a circuit from SEEs, three different levels of single event mitigation techniques can be applied, namely the system level, the circuit level, and the device level. For instance, Triple Module Redundancy (TMR) is one of the fault-tolerant approaches used at the system level that requires execution of three replication circuits, followed by a majority-voting process to produce an output. The disadvantage of the TMR approach is that these replication circuits consume more physical space (more than 200%) and power consumption. Developing in IC fabrication,

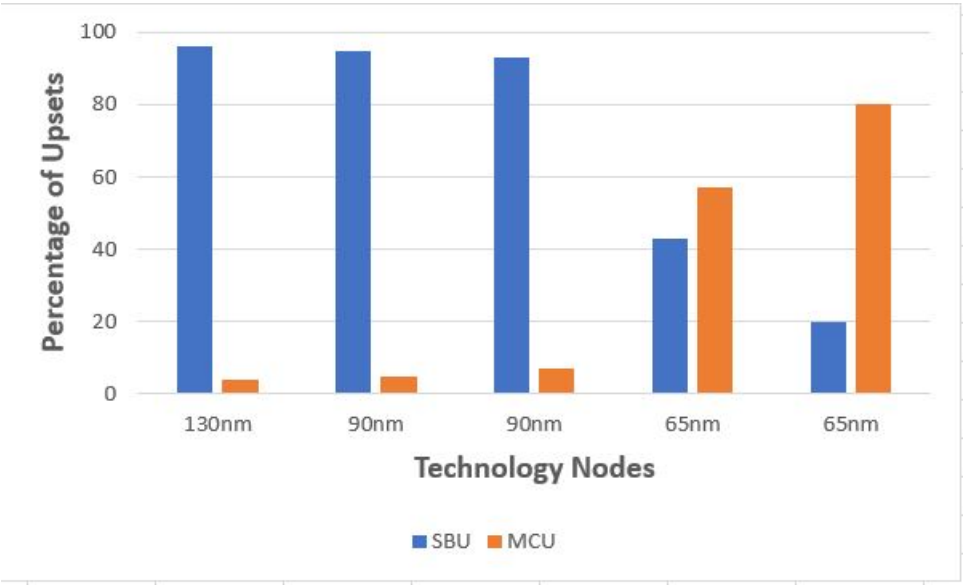



**Figure 1.3:** Percentage of SBUs and MCUs in different technology nodes [3]

such as Silicon On Insulator (SOI) instead of bulk technology, can improve the tolerance of an SEE at the device level [14]. To mitigate the SEEs at the circuit level, for instance, Dual Interlocked Storage Cells (DICEs) and Quad-node ten transistor cells (Quatros) are two SEU methods used in circuits [5]. They can be designed and applied in flip-flop cells or other storage blocks.

## 1.2 Motivation

As previously mentioned, the investigation of radiation effects has been evolving over decades. As shown in previous research the Fully Depleted Silicon On Insulator (FDSOI) technology effectively reduces the number of soft errors in a radiation environment compared to other ones, such as bulk or Partially Depleted Silicon On Insulator (PDSOI), on an SRAM element [15–17]. There are two unique innovations in FDSOI. First, there is a thin layer of buried oxide (an insulator layer) between the base silicon and the active area. Second, thickness of the source and drain diffusion areas is very small, so that the transistor can be fully depleted. Due to the thinness of the diffusion area, the gate

can control it efficiently, which results in lower power leakage. The 28nm FDSOI technology has several advantages, such as power and energy efficiency, and a wide operating voltage range. It can be applied to many applications requiring both low power and high reliability such as automobile and avionics.

Microprocessors incorporate multi-functions on a single IC. As the industry's leading supplier of microprocessor technology, Advance RISC Machine (ARM) has been supplying a processor based on reduced instruction set computing (RISC) architectures for a wide range of electrical applications [18]. It can be implemented in different areas, such as automotive equipment, smart cars, and sensor fusion. The ARM Cortex-M0 processor in ARM-M series is available to academic community, which satisfies the requirement in this project for a mitigated design on sequential logic and combinational logic with 28nm FDSOI technology. Because of the advantages mentioned above and because there has been little research on the radiation effects of 28nm FDSOI techniques for complex IC designs, this thesis focuses on experiments of SEEs on the 28nm FDSOI ARM Cortex-M0 and other electronic components. Various mitigation methods for ARM cores and flip-flop designs will be evaluated in the experiments in order to compare their performance in a radiation environment.

## 1.3 Objectives

Currently, with the more complex architectures and smaller size of circuits, and faster clock speed of processing elements, many variations of system-on-chip components have been implemented for use on earth and in the radiation of space. The SEE performance of these individual components such as logic gates, flip flops, SRAM, and clock trees with 28 nm FDSOI technology has

been studied and reported. Therefore, it is useful to examine SEEs on a complicated IC, in order to understand how such a chip performs in a radiation environment. A custom-designed test chip including several ARM Cortex-M0 cores, a TMR protected SRAM, and SEE-hardened flip-flops have been designed by former graduates in the research group. The ARM cores include combinational logic circuits, sequential logic circuits, and storage elements, all of which have different level of radiation sensitivities. It is an ideal platform to investigate the single event effects in a complex system with heavy ion experiments.

Considering all factors mentioned above, the research objectives of this thesis are as follows:

1. Develop a testing system including both software and hardware to evaluate the test chip in radiation experiments. The FPGA-based testing system based on Field Programmable Gate Array (FPGA) will be able to test the custom-designed IC chip combined with an ARM Cortex-M0 core, SRAM, and flip-flop (FF) chains in radiation conditions. The system can configure the chip to access to the FF chains and different mitigation types of ARM cores, and read back the experimental data during the test.

2. Measure and evaluate the radiation tolerance of SEE-hardened flip-flops implemented with the 28nm FDSOI. There are two FF chains integrated on the chip, the reference and the DICE FF chain. Compared with the result of the 28nm bulk experiment done in an earlier study [19], the number of soft errors which appeared in the 28nm FDSOI FF should be significantly reduced from that of bulk technology.

3. Analyze the SEE on SRAM implemented with the 28nm FDSOI technology. For the SRAM test, the individual SRAM blocks and the TMR mode of the SRAM will be tested in heavy ion experiments, to evaluate the effectiveness of the TMR method.

4. Measure and investigate the soft error rate for different mitigation levels of the ARM Cortex-M0 processor cores designed with 28nm FDSOI technology. Throughout the radiation experiment, the cross section of different mitigation types of ARM cores will be obtained and analyzed. In addition, the ARM cores will run with different clock frequencies to investigate the impact [20].

## 1.4 Thesis Organization

Beginning with the next chapter, the thesis is organized as follows:

In Chapter 2, the background of radiation effects will be introduced. First, the basic mechanism of a SEE is explained, followed by a discussion of experimental resources, such as pulsed laser resources and particle resources.

Chapter 3 describes the structure of the ARM chip that is to be tested, including the SRAM component, the configuration interface, and the different hardened architectures of the core.

Chapter 4 introduces the algorithm of the test system. First, it introduces the three main components in the system, namely the FPGA motherboard, the Raspberry Pi controller, and the DUT. Next, the design and setup of the SRAM test and the ARM core test will be described separately. In addition, this section also discusses software benchmarks.

Chapter 5 presents the results of the flip flops, the SRAM, and ARM cores subjected to heavy-ion testing. The cross-section value was analyzed and calculated, based on the experimental data. At the end of the paper is a brief overview of the test and some future tasks to be done in the future.

# 2 Basic Mechanism for Radiation Effects

## 2.1 Physical Origin of Single Event Effects

As mentioned in Chapter 1, when an energetic charged particle penetrates a sensitive region of a semiconductor material, it can lose energy and generate free electron-hole pairs along the track, as shown in Figure 2.1. This phenomenon can disturb the original state of the sequential logic, transiently disrupt the combinational logic, and even do permanent damage to the devices [21, 22]. There are two main processes that occur when an energetic particle travels through a device: one is charge deposition and the other is charge collection [4, 23, 24].

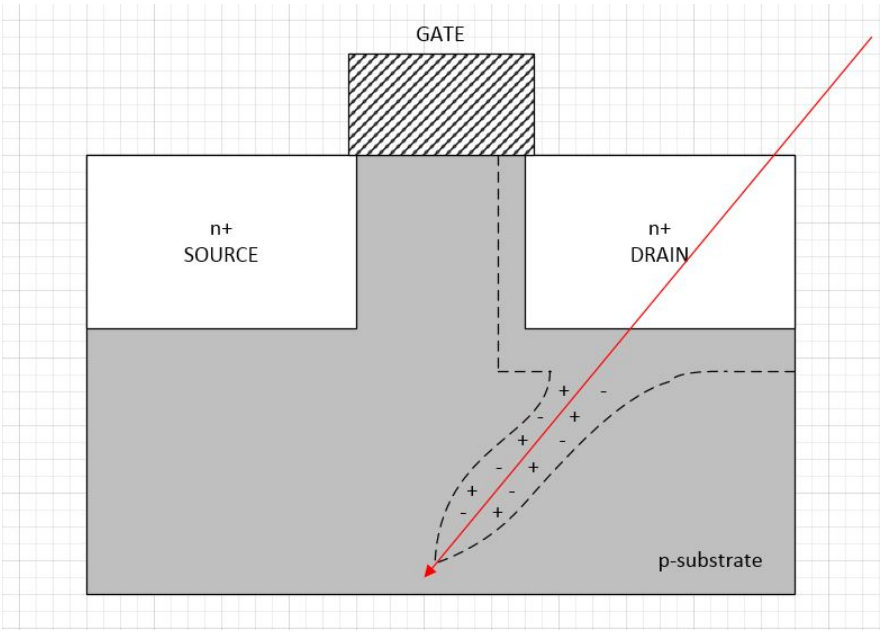



**Figure 2.1:** Particle track and free electron-hole parts in an MOS device

### 2.1.1 Charge Deposition

There are two fundamental effects when a particle passes through and generates a charge in a semiconductor transistor: direct ionization and indirect ionization [25, 26].

The reverse-biased PN junction is considered as the most sensitive region of a circuit affected by charged particles [27]. The main energetic charged particle, such as a heavy ion which is the nucleus of a heavy element, can cause an upset. In a radiation event, the particle transfers its energy to semiconductor materials as it is passing through it. A charged particle approaches or traverses the depletion region of the reverse-biased PN junction, along with a resulting funnel-shaped path of electrons and holes, and generates carriers immediately to produce a large current transient in that area [28]. The radius of this funnel-shaped track is usually less than one micron. The particle may rest or leave the substrate depending on its energy as shown in Figure 2.1.

In order to calculate the energy transferred from an incident particle to the materials, the linear energy transfer (LET) [29] is used. It is defined as the energy loss per unit length ($MeV/cm$) and is related to the density of the semiconductor material ($mg/cm^3$) Equation 2.1 is used to relate the two values. Thus, the unit of LET is $MeV \cdot cm^2/mg$.

$$LET = \frac{1}{\rho}\frac{dE}{dL} \tag{2.1}$$

There is a relationship between the LET of a particle and its charged deposition per unit length ($pC/\mu m$). Since the LET depends on the target material, and most of the ICs are designed and manufactured on a silicon wafer, it is well known that a charge deposition of 1 $pC/\mu m$ is equivalent to an LET of 97 $MeV \cdot cm^2/mg$ in silicon. The factor for converting between LET and charge deposition is almost 100.

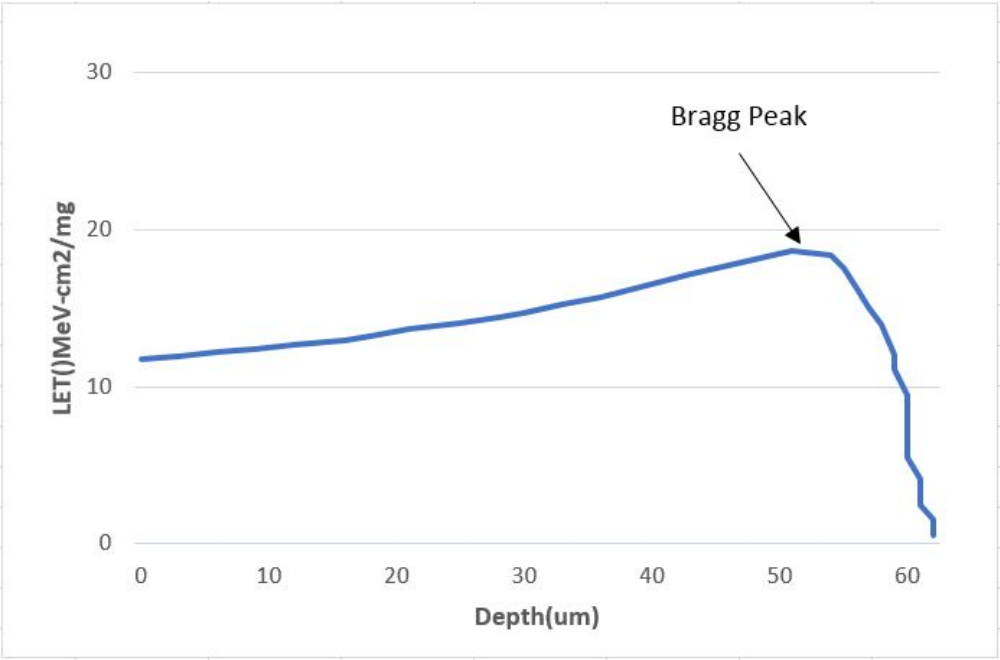



**Figure 2.2:** The curve of LET for 210MeV Chlorine ions in silicon [4]

Figure 2.2 shows a curve of the LET for a 210-MeV chlorine ion passing through a silicon substrate [4]. The energy loss per unit depth increase as the particle traverses, until it reaches an extreme point, called Bragg Peak. Subsequently, the particle will lose its energy quickly and eventually stops.

On the other hand, non-charged particles, such as neutrons, cannot cause ionization directly, but they can result in a SEE [30, 31]. Neutrons can produce circuit malfunctions by indirect ionization [4]. When a neutron enters the target material with high energy, it may collide with a target nucleus to produce charged secondary particles, and these reaction products can cause direct ionization, as described above.

### 2.1.2 Charge Collection

Charge collection can be contributed to by two processes, drift and diffusion [32,33]. At the beginning of an ionization event, an energetic particle approaches a node of a transistor and forms a high concentration of carriers around it [27]. Figure 2.1 shows an illustration of radiation occurring at a N-channel Metal Oxide Semiconductor (NMOS) transistor. The original depletion region between the drain and p-substrate is distorted to form an extra funnel shape along the ion's trajectory. This high funneling electric field can collect electrons in or around the depletion area efficiently and sweep them into the drain region swiftly due to drift. The drift process produces a large transient current and finishes within hundreds of picoseconds. The unexpected voltage/current perturbation can be captured or change the state of this logic point, then cause a soft error. Another charge collection phase is diffusion, which becomes a dominating process after drift, and will last for a longer time, up to hundreds of nanoseconds [27]. During this period, all free electrons and holes are collected, recombined, or diffused away from the depletion region. The theory of charge collection in P-channel Metal Oxide Semiconductor (PMOS) is approximately the same as in NMOS. Because the N-well of PMOS is enveloped by the p-substrate,the direction of the electric field between the drain and N-well, and between the N-well and p-substrate are opposite. When a radiation event occurs, excess holes can be swept into the drain between the area of the drain the and N-well. At the same time, holes which are freed near the p-substrate are repelled toward the opposite side since the direction of the field is toward the p-substrate. This phenomenon can cause the charge collected by a PMOS transistor to be less than the charge collected by an NMOS transistor.

## 2.2 Major Division of Single Event Effects

Single Event Effects (SEEs) caused by a single energetic particle can create serious negative effects in ICs [34]. There are two main errors due to SEEs [35]. The first type of error is called a "soft error," which is a temporary non-destructive error that can be recovered and does not introduce permanent failures. The second type of error, called "hard errors," result in permanent system failures.

### 2.2.1 Single Event Upset (SEU)

There are two main categories of digital circuits, sequential logic and combinational logic. The outputs of sequential logic circuits depend not only on the current inputs, but also by the current state. In another words, sequential circuits must have memory elements to store the previous data. The basic transistor-level schematic of a D-flip-flop (DFF) is shown in Figure 2.3. It is the most basic register element in an IC design. It contains two serial latches and is controlled by two transmission gates [36]. There are two back-to-back inverters in each latch to restore 1-bit of data (1 or 0). When the clock is logic low, transmission gate 1 and 4 in Figure 2.3 are open. The input data propagates into the first latch, but cannot pass to the next latch because gate 2 is closed. During this period, the second latch still holds the previous data until the clock signal has been turned to logic high. Once the rising edge of the clock signal arrives, the gates 1 and 4 are turned off at the same time as gates 2 and 3 are turned on. In this condition, data can be locked in the first latch, and transferred to the next latch no matter how the input data changes. Stable output data is also available at this moment.

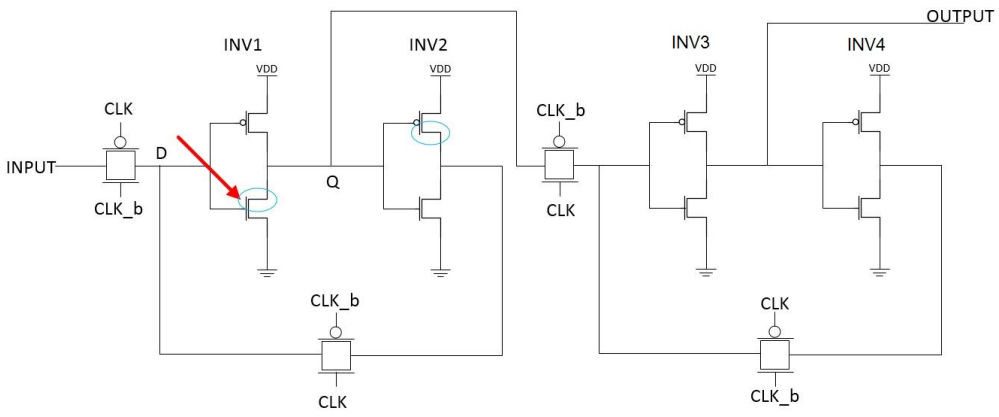



**Figure 2.3:** Transistor-level schematic of D-flip-flop

The basic DFF working process is described above. If the setup/hold time is satisfied, the DFF should store the data constant by the circuit. However, if an energetic particle strikes at a sensitive node, such as the blue-circle of regions in Figure 2.3, it might cause a bit flip. In this situation, the critical charge ($Q_c$), which is defined as the minimum total of charge collected to upset the data in this storage element, is an important parameter to evaluate whether the logic value has been upset [37]. As shown in Equation 2.2, critical charge equals to the product of total capacitance of the transistor node ($C_n$) and the voltage of the power supply ($V_{dd}$).

$$Q_c = C_n \times V_{dd} \tag{2.2}$$

If the radiation event induces an SEU, that indicates the charge collected at the sensitive node is greater than the critical charge, the data locked in the first latch, for instance, is 0 (D=0, Q=1), when the clock signal is logic high. In this case, the PMOS of INV1 and the NMOS of INV2 are closed. The NMOS of INV1 and the PMOS of the INV2 are open at meantime, which means both of drains, marked by the blue circles shown in Figure 2.3, are reverse biased. If an energetic ion hits the NMOS drain area of INV1, indicated by the red arrow in the figure, a current pulse occurs

at this sensitive node during the period of charge collection. If the current pulse is large enough, the logic value of Q can be driven to 0. The data stored in this latch would be upset totally (D=1, Q=0), because this type of feedback structure can hold the wrong data until the next clock falling edge. This phenomenon called an SEU, and the possibility for an SEU to occur in a storage cell is referred to as a "cross section." The cross section ($\sigma$) can be considered as the total errors in one device ($n$) divided by the particle fluence ($N$), as shown in equation 2.3, and it is expressed in $cm^2$ [37].

$$\sigma = n/N \tag{2.3}$$

Failure in Time (FIT) is another common unit used to measure the Soft Error Rate (SER) [38]. One FIT represents a one-time failure in one billion device hours. For example, if a single chip system FIT value is 1000, that means this system would have one failure per 114 years [39]. FIT is equal to $\sigma \times \phi \times 10^9$, where $\phi$ is the fluence of a particle in the environment ($n/cm^2/h$).

### 2.2.2 Single Event Transient (SET)

Compared with the sequential circuits, combinational circuits are composed of logic gates whose output depends only on the input at the present time [39]. In Figure 2.4, the combinational logic cloud is filled with a variety of logic gates without storage elements. If a radiation event induces a charge collection in any logic gate, it might cause a transient voltage pulse, which could be captured in a subsequent register [40, 41]. This phenomenon is called a Single Event Transient (SET).

Generally, this momentary SET glitch does not necessarily induce contaminative data. There are three different masking mechanisms, namely logic masking, temporal masking, and electrical

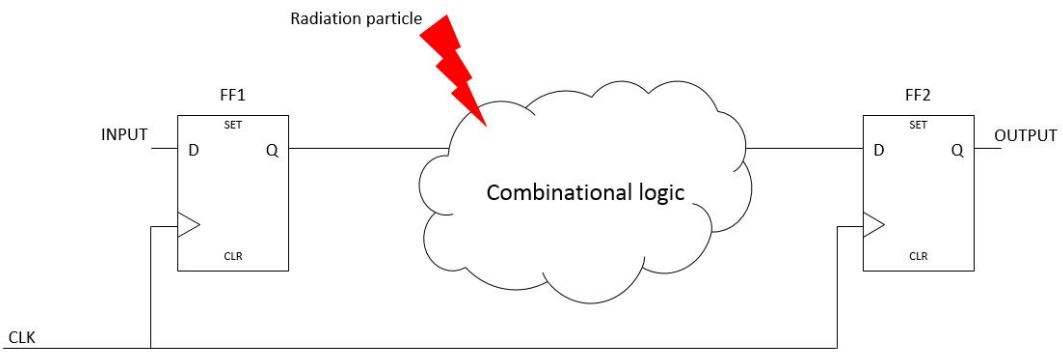



**Figure 2.4:** Simple structure of a combinational logic circuit

masking, which could mask out the SET pulses [39].

Logic masking refers to the occurrence of a SET pulse propagating through an insensitive logic path, which cannot change the final output state. For instance, suppose there are two inputs, A and B, passing through a two-input NAND logic gate. If the state of input A is logic low, the output of the NAND gate is logic low regardless of the state of input B. At this moment, if an incident particle strikes the B node of the NAND gate transistor, inducing a SET pulse at input B, the output result of the logic gate would not be affected, because input A masks the radiation event.

When there is a SET pulse generated in combinational logic, but the pulse is not sampled by the following register, it is referred to as temporal masking [42]. As shown in Figure 2.5, the input signal representing the result from a combinational logic as an input to the register (DFF), has a positive SET pulse. If the clock for the DFF is CLK1, the SET would be sampled as the clock rising edge arrives, and the fault result is stored in the DFF. However, if the DFF clock is CLK2 in Figure 2.5, the glitch will not be sampled. In this situation, the SET pulse is overridden by the temporal masking. The third masking mechanism, electrical masking, means that the SET pulse is narrower than the logic gate propagation delay, so that the pulse is eliminated during signal propagation [39].

Experiments by Buchner et al. illustrate the error rates caused by SEUs and SETs, and the re-

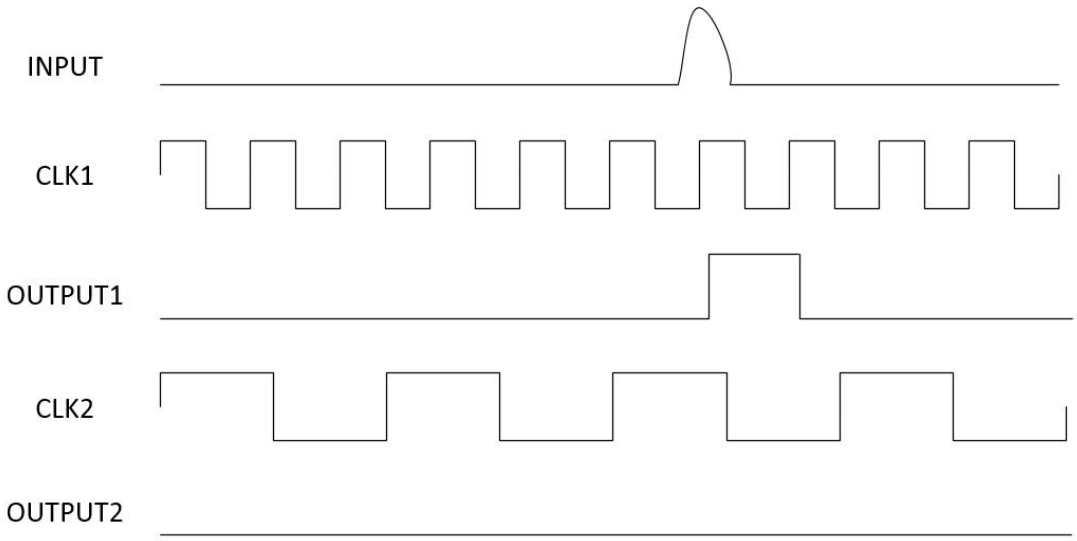



**Figure 2.5:** SET of two different types of clock frequencies

lationship between them [20]. A simple combinational element (inverter) and a sequential element (D-latch) were combined in the test circuit for examination at different frequencies. The results demonstrated that the SER from SEUs remained at the same order of magnitude as the frequency increased, while the SER from SETs increased linearly. It is foreseeable that soft errors caused by SETs may become dominant in the future due to the development of high speed technologies.

## 2.3 Mechanism of Radiation Experiments

An electrical device working in a cosmic environment is confronted by the reliability issues, which can be caused by two major radiation sources, galactic cosmic rays and solar activities. Irradiation experiments on the ground, using particle accelerators or pulse laser facilities that simulate the effects of energetic particles in the natural environment, have become increasingly significant for investigating and studying the reliability of IC designs.

### 2.3.1 Pulse Laser Resource

Pulse laser tests have been applied to investigate SEEs for a couple of decades, since photons can also ionize atoms by releasing electrons [43]. Different from Coulomb interaction used in particle liberating the electron-hole pairs due to the energy and number of ionizing atoms, there are three cases when photons generate electron-hole pairs: the photoelectric effect, Compton scattering, and pair production [44]. Recently, increasing SEE research activities based on lasers can be attributed to three factors. First, the sensitive area for a SEE can be located precisely by the spatial information from the control part of laser facilities. Second, the laser does not damage the circuits physically. Third, experiments at particle accelerator facilities are much more expensive and it is difficult to book access to the equipment [45]. But these is an alternative method to investigate radiation effects. By injecting a pulse laser into the specified sensitive node, it is easy to control the spot where the transistor needs to be tested and observe the SEE response of the device under test (DUT). In view of the above factors, the early motivation for using a laser test is to simulate SEEs in ICs and provide some advance information before performing the experiment in particle accelerator facilities.

Single-Photon Absorption Lasers (SPAs) and Two-Photon Absorption Lasers (TPAs) are two types of pulse laser resources [46, 47]. The SPA requires that the energy of photons should be greater than that of the semiconductor bandgap, whereas the wavelength of the laser should be shorter than a specific constant. For instance, the bandgap of silicon is $1.12eV$, so the wavelength should be shorter than $1108nm$. If nonlinear absorption effects are ignored, the energy can be absorbed directly, and produce electron-hole pairs. The equation from irradiance, $(I(z))$, is shown below, where $I_0$ is the irradiance at the surface of the material, and $z$ is the depth of the photon

traversing below the surface. The attenuation coefficient, $\alpha$, is related to the wavelength of the laser ($\lambda$).

$$I(z) = I_0 e^{-\alpha(\lambda)z} \tag{2.4}$$

As the name of TPA suggests, if the photon energy is less than the energy of the semiconductor bandgap, electon-hole pairs can also be generated via absorption of two photons simultaneously. If TPA is the dominant process, the irradiance can be solved by

$$I(z) = \frac{I_0}{1 + \beta(\lambda) I_0 z} \tag{2.5}$$

where $\beta(\lambda)$ is the two photon wavelength-dependent absorption coefficient. Compared with SPA, TPA is more benefit in SEE research. Since the energy of SPA decays exponentially once attached to the surface and the wavelength of TPA is longer than SPA, TPA has a better penetration and less attenuation than SPA. To avoid damaging the dice physically from the front side, TPA can be applied using back-side irradiation. Many TPA pulse laser facilities are established globally, such as the U.S. Naval Research Laboratory (URL) and the Saskatchewan Structural Sciences Centre (SSSC) located at the University of Saskatchewan to facilitate SEE research.

Figure 2.6 shown the SCCC laser facilities which is divided into two main sections, an amplification stage and a post-amplification stage. Laser power, wavelength, and repetition frequency can be regulated in the former stage, while the components of the test system can be configured and monitored in the latter stage.

On the other hand, because of fundamental differences between SEEs caused by pulse lasers and energetic particles, a TPA laser test cannot substitute completely for particle hits. However,

use of lasers appears to provide a prediction or simulation for the next stage of particle hits.


**Figure 2.6:** Pulse laser facility at SSSC, in University of Saskatchewan

### 2.3.2 Particle Resources

As briefly mentioned in Chapter 1, many particles, such as alpha particles, protons, heavy ions, or neutrons, in cosmic or terrestrial circumstances can cause SEEs. Various particle accelerator facilities are widely utilized around the world to simulate a radiation environment. These facilities can provide various types of particles for SEE experiments.

Heavy ions are those energetic charged particles, whose atomic number is greater than one, such as carbon, neon, or calcium. A heavy ions can free electron-hole pairs along its track via direct ionization. Both cyclotrons in Lawrence Berkeley National Lab (LBNL) and the RADEF facility in the Accelerator Laboratory at the University of Jyväskylä can provide heavy-ion beams in different ion cocktails for use in testing. The range of LET of heavy ions is normally from 1 $MeV \cdot cm^2/mg$ to 100 $MeV \cdot cm^2/mg$.

Since their percentage exceeds 85% in cosmic rays, protons are another common radiation resource that cause SEEs. In general, researchers believe that the high energy of protons cause upset in memory cells via indirect ionization, which leads to the generation of soft errors. However, there is growing evidence that proton-induced direct ionization also might occur [48]. If the energy of a proton is less than 10MeV, it can induce the electron and hole pairs directly. TRIUMF laboratory at the University of British Columbia is the available facility for proton testing in Canada.

### 2.3.3 HI-13 Tandem Accelerator

In addition to the laboratories mentioned in the last section, there is a particle-acceleration facility at the China Institute of Atomic Energy in Beijing, China. It is an HI-13 Tandem Accelerator [49], and a heavy-ion radiation experiment of the ARM-M0 was conducted there. The irradiation facility is shown in Figure 2.7.

This facility is specifically configured to conduct SEE ground tests of semiconductor devices and circuits. The size of the Devicce Under Test (DUT) platform is the same as the one at Brookhaven National Laboratory in the United States, which can accommodate multiple DUT boards at the same time. The technology of two-dimensional asynchronous magnetic scanning is used to scan the original beam spot into a large, uniform beam spot. In order to monitor the beam flux, there are four detectors around the beam spot for continual measurement. The advantages of this feature are that it can monitor the irradiation flux without affecting the beam energy and can supervise the distribution of the beam spot in real time. The entire beam line facility is designed as a multi-level vacuum gradient, which ensures that the irradiation target chamber can be implemented with the accelerator if the vacuum value reaches $10^{-2}Pa$. It reduce the waiting time for vacuum pumping the air, and thus will improve the efficiency of the experiment.

**Figure 2.7:** The Single Event Effect irradiation facility in the HI-13 Tandem Accelerator

The HI-13 Tandem Accelerator can provide more accurate experimental data from shapely rising area in the cross-section curve. In addition, using the common range of LET values in Single Event Effects, researchers at irradiation facility in the HI-13 Tandem Accelerator also investigated some commonly used ions, such as Ge and Ti. The process can achieve one or more complete cross-section curves of a SEE in about 20 hours on the HI-13 Tandem Accelerator SEE irradiation device.

# 3 ARM Core Test Vehicle Modular Description

As mentioned in earlier sections of this thesis, different types of SEEs can induce errors in devices or electronic components, which can lead to serious accidents. A good approach to study radiation effects is to apply a mitigation design to circuits and then test these using different particle resources on the ground. The ARM Cortex-M0 is a basic microprocessor which consists of numerous sequential and combinational logics. Applying a mitigation design to the ARM can help us to study a SEE on a complicated circuit. This chapter will introduce different components in the ARM chip. The ARM M0 test chip was designed in collaboration with the University of Saskatchewan, Carlos III University of Madrid, IROC Tech and Cisco Systems.

## 3.1 Top-level Description of the ARM

To study the impact of an SEE on different hardened levels of processors, four variants and one reference of the ARM Cortex-M0 cores were designed and implemented on a die.

The Cortex-M0 processor is a 32-bit Reduced Instruction Set Computing (RISC) processor and is equipped with a von Neumann architecture shared memory for programs and data. There are register banks, an arithmetic logic unit (ALU), a data path, and a control logic contained in a processor core. The total number of flip-flops in one core is 840, and the area consumption in the

28nm FDSOI library is approximately 17,000 $\mu m^2$. To research hardened flip-flops and hardened combinational logic gates working in a radiation environment, the five variant cores shown in Table 3.1 are used.

| Number | Name | Description |
|---|---|---|
| 1 | Reference Core | Original FF, and original combinational logic gate |
| 2 | Mitigation FF Core | DICE FF, and original combinational logic gate |
| 3 | Mitigation Logic Core 1 | DICE FF, and low-effort hardened combinational logic |
| 4 | Mitigation Logic Core 2 | DICE FF, and medium-effort hardened combinational logic |
| 5 | Mitigation Logic Core 3 | DICE FF, and high-effort hardened combinational logic |

**Table 3.1:** ARM Cotex-M0 variant

The first core is designed as a reference for blank control and is implemented with normal combinational logic and conventional flip-flops. It provides a baseline to compare with the others. The second ARM core is designed using DICE flip-flops, normal combinational logic, and a clock tree. This DICE variant should provide good performance on SEUs. In addition, it serves as a baseline for the combinational sensitivity. The combinational logic of the remaining three variant ARM cores is substituted and protected by increasing the approximate combinational logic from low to high level.

In addition to the five variant cores, there are three other functional blocks, namely, two FF

chains interfaces, control logic on-chip memories, and an on-chip clock generator on the die. One of the chains is a regular flip-flop chain, and the other is a DICE architecture flip-flop chain. All five ARM cores share one memory block, which can be configured into five different modes. The memory block can be operated as three individual memories which contain 4KB in each section. The other two modes, which are Triple Module Redundancy (TMR) mode and depth mode, manipulate the entire memory block to store programs or data. TMR is a mitigation technique used at the system level for hardening memory. The input data will be copied three times and stored into three memory sections. When reading this data from the memory, a majority vote is performed between the three copies to decide the output data. In other words, the TMR memory has the storage capacity of 4KB. In the depth mode, the three memories are combined and expanded as a $3 \times 4$ KB memory, and the two higher address bits control which 4KB RAM is selected. The clock is provided by the on-chip clock generator, which uses a programmable ring-oscillator to generate the clock. This ring-oscillator can provide a maximum clock frequency of approximate 1 GHz, and is designed in steps of approximately 50MHz down to 200MHz. Figure 3.1 shows the floor plan of the entire test chip.

## 3.2 Communication Interface

This section describes the communication interface of the test chip, including the configuration block, status block, and control block. The basic concept and architecture are illustrated in Figure 3.2. The test chip needs to be configured in several areas, such as the selection of the testing core, operation frequency, and test program. The program and writing address are also transmitted from the control system to the test chip and stored into the SRAM on chip. After the programming is

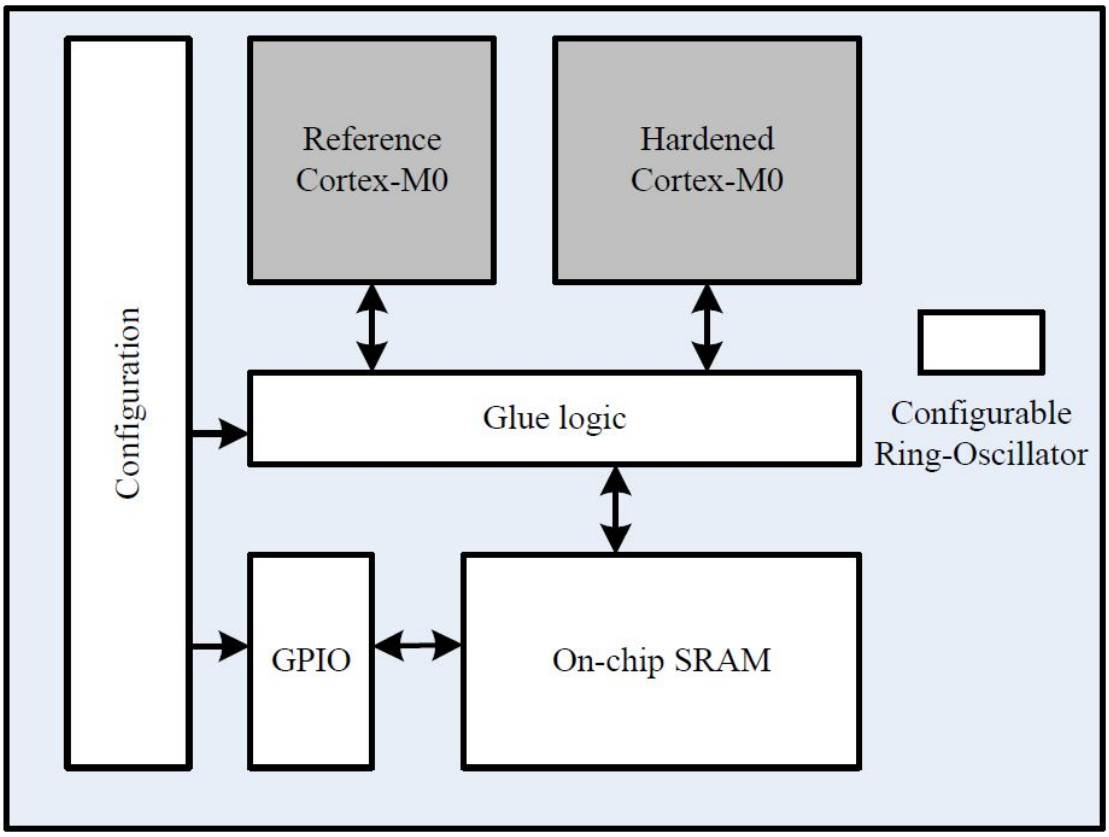



**Figure 3.1:** The schematic of the test chip

done, the result or error data can be submitted from the status interface for analysis. The control block in Figure 3.2 configures the test chip using the configuration interface and communicates directly with the SRAM.

### 3.2.1 Configuration Section

As a configurable test chip, the configuration interface is used to initialize the function of this chip. The possible functions include writing data into SRAM, selecting clocking modes, or the choice of core to be tested. The schematic diagram of the configuration interface is shown in Figure 3.3.

The serial data (CONF_DATAIN) contains 128 bits of input data and is protected with an odd parity bit in every 16 bits. As a result, the sum of the serial configuration data in 136 bits. In other

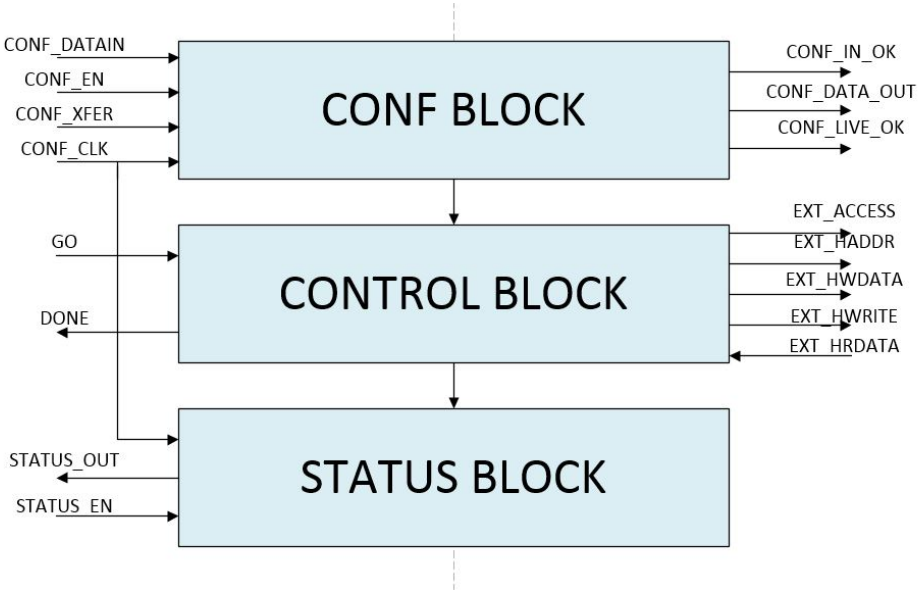



**Figure 3.2:** The schematic diagram of the transmit and receiving block

words, the configuration data is divided into eight groups, including 16 bits of data and one parity bit. The parity checkers are used to check the elements in each group, and the output of each checker should be a logic high. All outputs of checkers pass through an AND gate to confirm that the data stored in the serial configuration input interface is correct. When a control signal (CONF_XFER) has been asserted, data in the block of living configuration is updated simultaneously from the serial configuration input interface. When the process of new configuration data is loading, the current configuration block keeps the latest data stable.

The architecture of the serial configuration input is illustrated in Figure 3.4. As shown in the figure, every bit of data shifts into three copies of the flip-flop chains on the rising edge of the configuration clock during the period when the enable signal (CONF_EN) is asserted. In this way, 136 bits of input data, including parity bits, can be transmitted completely into the serial configuration input block. In the next step, the enable signal (CONF_EN) is de-asserted (logic low), and at the same time the contents of each stage are checked and locked by the subsequent

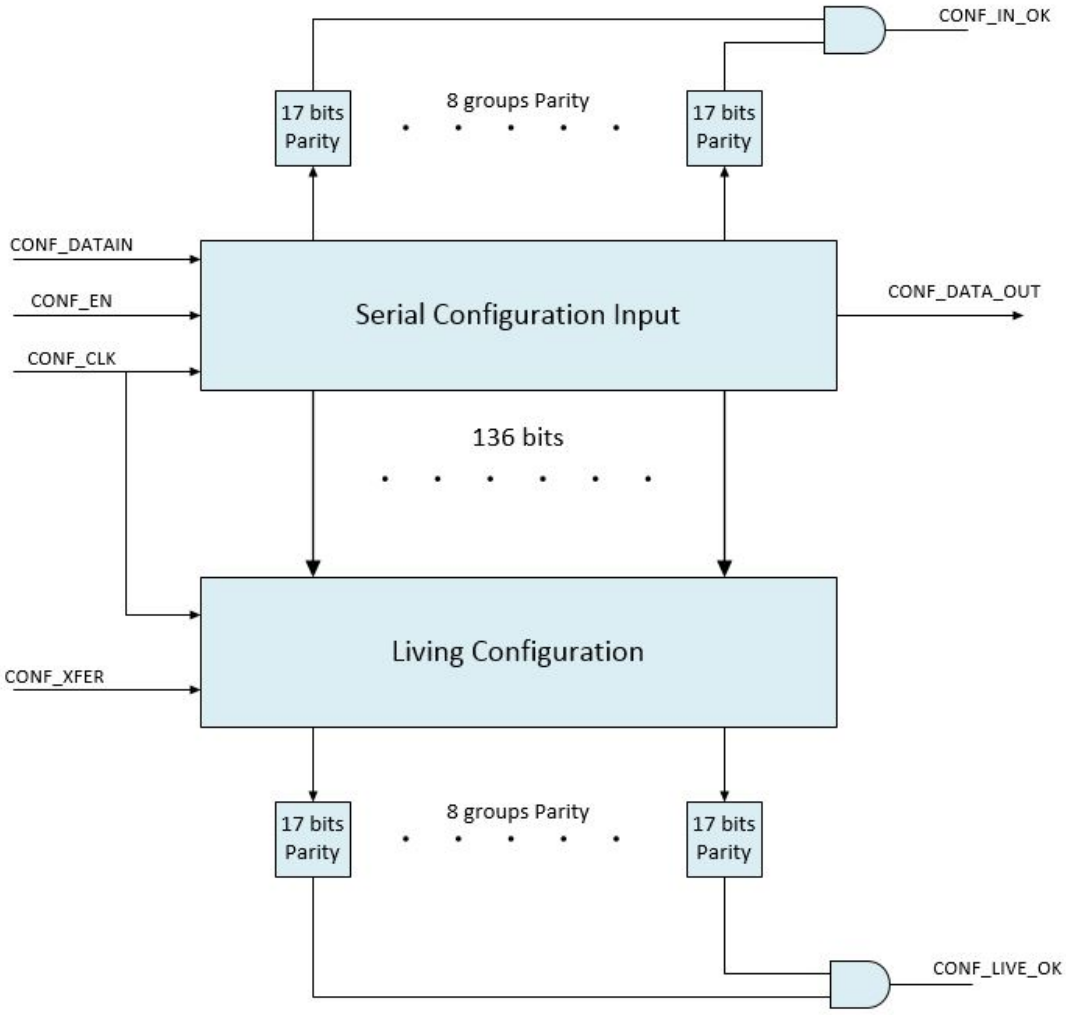



**Figure 3.3:** Schematic diagram of the configuration interface

TMR voter.

When the two enable signals (CONF_XFER_A and B) are asserted, the configuration data is copied from the serial configuration data block to the living configuration data block in parallel. If the two signals are not asserted at the same time, the living configuration is stored in a loop circuitry. Three independent voters are used to determine the data for each copy, as shown in Figure 3.5. An error occurring in a register can be corrected, and it cannot cause permanent damage.

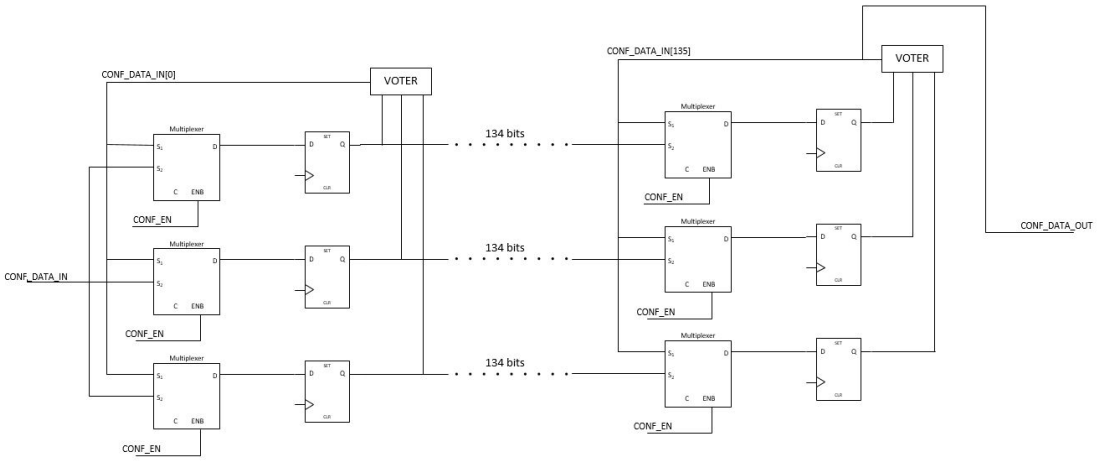



**Figure 3.4:** Schematic diagram of serial configuration input

### 3.2.2 Status Interface

In addition to the configuration interface, serial interface is also used to transmit 48 bits of status information, including reading data from the SRAM chip memory. The same as in the configuration section, the status information is also protected by an odd parity for each 16 bits of data, and the parity can be checked by the control system (FPGA).

The role of the status interface is similar to that of the configuration interface, except that the purpose of the status interface is to transfer information back to the FPGA. The communication clock of the status interface is shared with the configuration clock, however, an independent enable signal (STATUS_EN) is triggered when a serial transmission is performed. There are two blocks to store status information, that is, the live status information and the transmission information, as mentioned in the configuration section. If STATUS_XFER_A and STATUS_XFER_B are logic high on the rising edge of the configuration clock, the live status information can be copied to the serial transmission block. The status information can be shifted out bit by bit on the rising edge of configuration clock when the STATUS_EN is asserted (logic high).

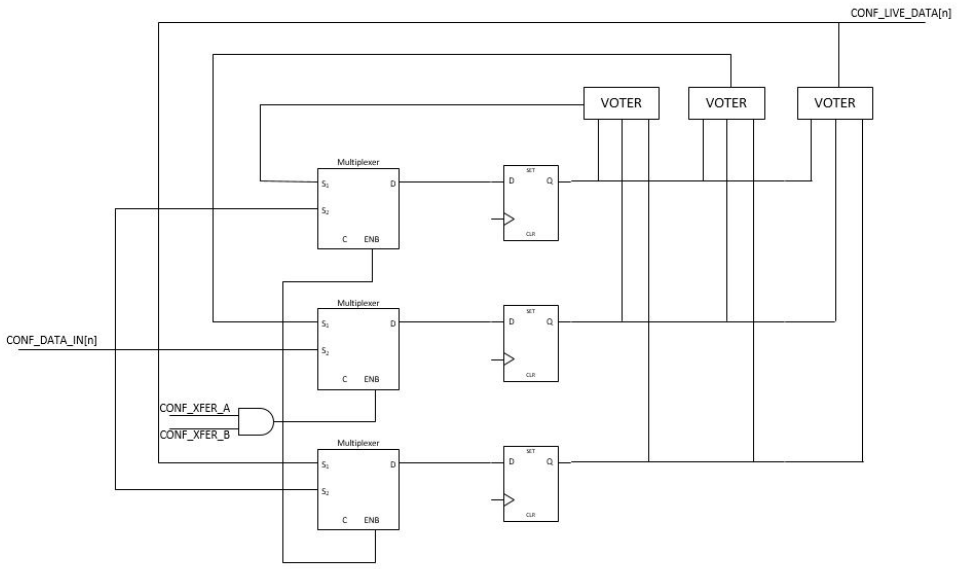



**Figure 3.5:** Schematic diagram of the living configuration interface

### 3.2.3 Control Commands

As mentioned at the beginning of this section, the test chip can be configured using control commands through the configuration interface, and it submits the status information back to the testing system through the status interface. Each command has 76 bits and contains the fields shown in the Table 3.2.

| Field | Bits | Description |
|---|---|---|
| Command | 4 bits | Includes 8 different operations |
| R_Addr | 12 bits | Reading address |
| Data | 32 bits | Writing data |
| W_Addr | 12 bits | Writing address |
| Len | 16 bits | Number of operations |

**Table 3.2:** Structure of the operation commands

There are eight different commands shown in Table 3.3. The controller can decode the commands with different arguments and instruct the processor to execute them. The controller does not do anything in the idle state, which correspond to 4 bits of zero. The data in the R_Addr address can be read out and sent to the status interface in the read state. For the write state, the controller can write data into the W_Addr address of the on-chip memory. The fourth command instructs the controller to fill a certain length of data starting at the W_Addr address into SRAM. The checksum state is the next command, which can calculate the value of checksum for a certain length of words starting at the R_Addr address. The sixth command is to copy a certain length of data starting from the R_Addr address to the W_Addr address. In the scrub state, the test chip performs a TMR read and write process from the R_Addr address from deep of Len. The last command is to execute the program on one of the test cores.

| Command | R_Addr | Data | W_Adrr | Len |
|---|---|---|---|---|
| IDLE:4'D0 | | | | |
| READ:4'D1 | √ | | | |
| WRITE:4'D2 | | √ | √ | |
| FILL:4'D3 | | √ | √ | √ |
| CHECKSUM:4'D4 | √ | | | √ |
| COPY:4'D5 | √ | | √ | √ |
| SCRUB:4'D6 | √ | | | √ |
| RUN:4'D7 | | | | √ |

**Table 3.3:** Contents of on-chip command

After a line of command is transferred into the configuration interface, the test system sends a

"GO" signal, informing the controller that the transmission has been completed. Then the command is analyzed and executed. When the execution of the command has been finished, the "DONE" signal is asserted to inform the test system to carry out the next stages.

## 3.3 Clock Generator

The clock generator is one of the most important and irreplaceable function blocks in the processor. As a common digital test chip, this experiment on the ARM M0 processor also requires a testing clock to implement the test program, and it is equally essential to make the clock frequency variable. In order to comprehend the relationship between a SEU and a SET, observing the testing consequence under different levels of clock frequency is an effective method to implement SEE experiments.

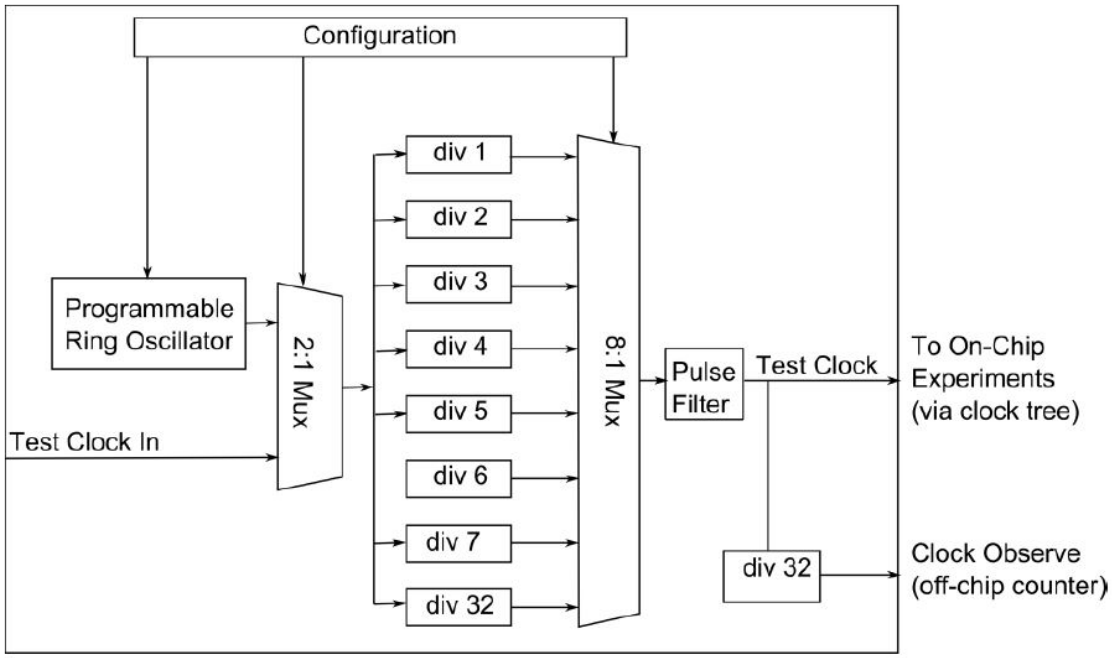



**Figure 3.6:** High-level circuitry for clock generator

There is a programmable ring oscillator (RO) implemented on-chip to generate the clock. The

circuitry of the clock generator is shown in Figure 3.6. As illustrated, the programmable RO is not the only source for the clock. In addition to the on-chip clock generator, there is an input port to receive an external clock which can be used for the experiment, and these two options can be configured by the configuration interface.

In addition to selecting the clock source, the configuration interface also selects the test clock division factor as one of 1, 2, 3, 4, 5, 6, 7, or 32. The option of 32 is a special one which enables the test system to operate in a low frequency situation. The impact of a SET is greater than the a SEU as it decreases the operating frequency.

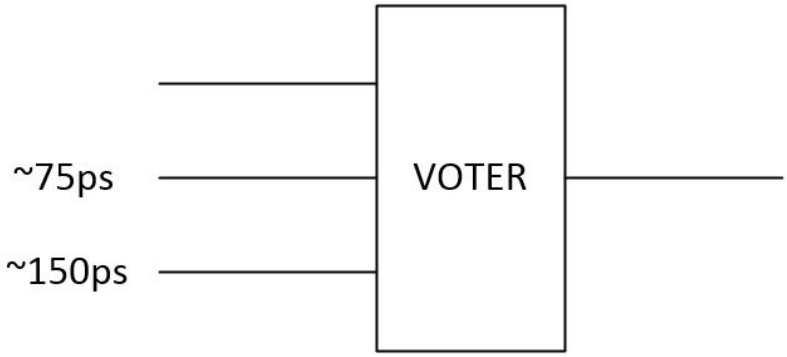



**Figure 3.7:** The architecture of a pulse filter

In order to protect the clock generator in a radiation environment, the circuitry has been mitigated with two hardening techniques to reduce the errors from SEE. First, the inverters are designed to be as large as possible. There are two reasons to use large cells to design the clock component. A larger cell can reduce the sensitivity of single event transient effects, and it also has a higher inertial delay, which is a natural filter for the transients. If a short transient occurs at the input side of an inverter, it can be eliminated at the output.

The second hardening method is to apply the Pulse Filter technique to filter the transient pulses. If a transient occurs before the Pulse Filter and its given width is less than the filter's delay, this transient can be blocked by the filter. The architecture of a Pulse Filter is illustrated in Figure 3.7.

For calibration purpose, the clock frequency can be observed through an output port. The programmer or tester can test the chip's working clock frequency effortlessly through this pin (CLK_OBS_OUT). The output signal of CLK_OBS_OUT comes from one of the four clock sources, which are a local ring-oscillator divided by 32, an external clock source, a selected Vernier detector, and a selected classic detector. By dividing the local clock by 32, the waveform is presented clearly and accurately on the oscilloscope's screen.

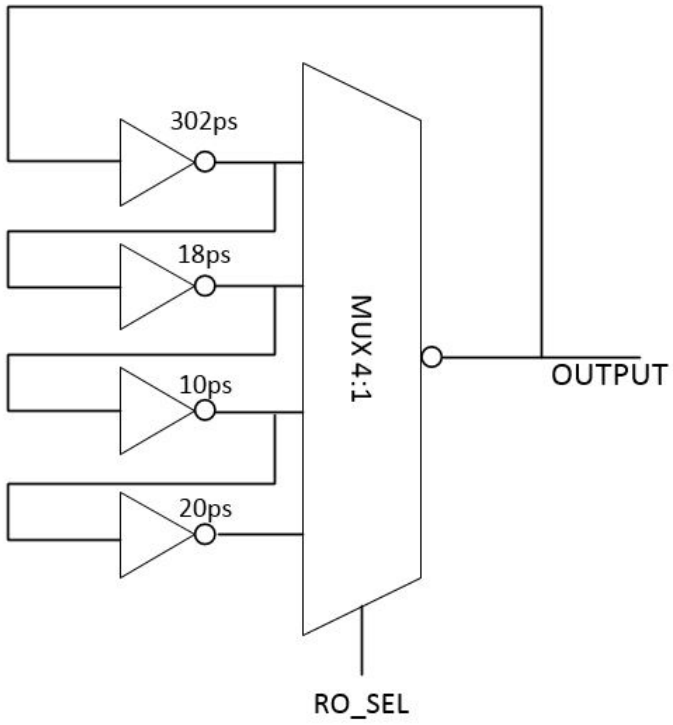



**Figure 3.8:** The Architecture of a Programmable Ring Oscillator

The architecture of a programmable RO is illustrated in Figure 3.8. A nominal delay of 302ps is the initial delay chain for the test chip. In addition, there are three different increment levels of

delay which can be configured by the control bit (RO_SEL) through a 4:1 MUX. Combined with the clock frequency divider mentioned above, these two components produce a wide range of test frequencies for the chip in the test. Table 3.4 shows the different clock frequency configurations.

| RO DELAY | DIV1 (MHz) | DIV2 (MHZ) | DIV3 (MHz) | DIV4 (MHz) | DIV5 (MHz) | DIV6 (MHz) | DIV7 (MHz) | DIV32 (MHZ) |
|---|---|---|---|---|---|---|---|---|
| 302ps | 3311 | 1655 | 1104 | 828 | 662 | 551 | 473 | 104 |
| 320ps | 3125 | 1562 | 1041 | 781 | 625 | 520 | 446 | 98 |
| 330ps | 3030 | 1515 | 757 | 757 | 606 | 505 | 432 | 95 |
| 350ps | 2857 | 1429 | 952 | 714 | 571 | 476 | 408 | 89 |

**Table 3.4:** On-chip clock frequency of ARM-M0 chip

The values of the clock frequencies come from the simulations; the clock frequencies in the test chip are different from the simulation result due to manufacturing factors. During the experiments, the clock frequencies selected in the ARM cores are from 100 MHz to 600 MHz, within which the ARM cores can work successfully.

## 3.4 SRAM Specification

This section introduces the functionality and implementation of the SRAM to be applied as a storage device for the ARM-M0 cores. This SRAM includes these identical pages, each of which has $256 \times 4$ words. The word width of this SRAM is 32 bits. Depending on the user-defined configuration, the SRAM can operate in one of the following five modes:

- Only the first page is accessed;

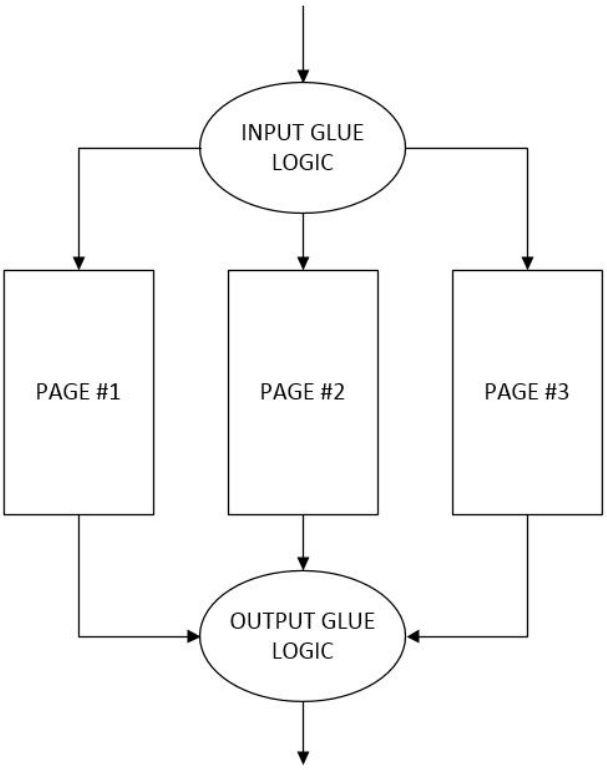



**Figure 3.9:** Diagram of SRAM

- Only the second page is accessed;
- Only the third page is accessed;
- TMR mode of three pages; or
- All three pages are accessed (depth mode).

Each page has an identical architecture while the configurations above are implemented through the glue logic outside of the three pages. The overall diagram of the SRAM is illustrated in Figure 3.9. The SRAM component is expected run at a 500MHz or higher clock frequency.

The conventional 6-transistor (6T) cell is applied as the bit-cell. The schematic of the 6T bit-cell is illustrated in Figure 3.10.

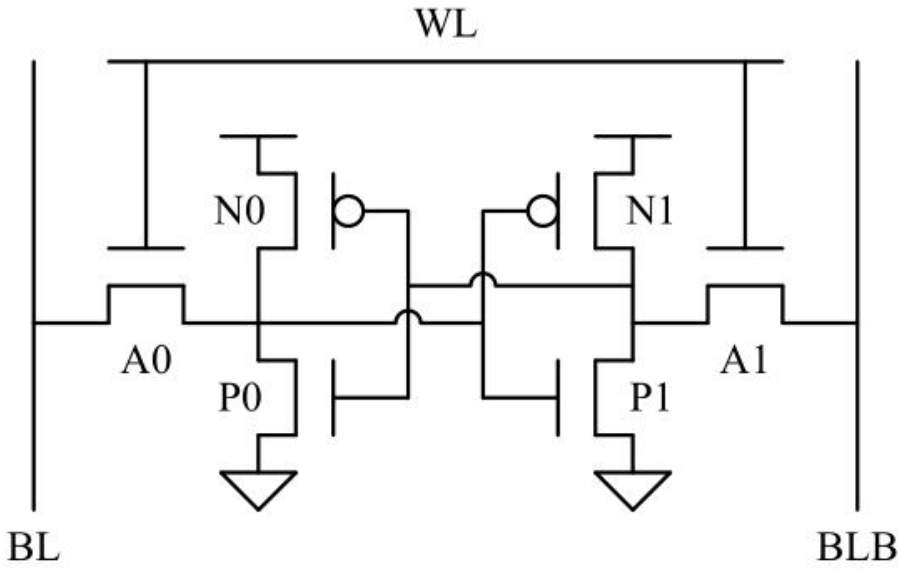



**Figure 3.10:** 6T bit-cell

The operation timing of the SRAM is compatible with the Advanced Microcontroller Bus Architecture (AMBA) Advanced High-performance Bus (AHB) protocol. The read and write timing of this protocol are illustrated in Figure 3.11. The timing of control signals and corresponding address signals are the same, while the read and write data are delayed by one cycle. As shown in Figure 3.11, for a write operation, the ARM-M0 core asserts the control signal and address of the HADDR port in Cycle 0 and then asserts the write data on HWDATA in Cycle 1. For a read operation, the ARM-M0 asserts the corresponding address signal of the same HADDR in Cycle 2, and the SRAM should provide the readout data on HRDATA in Cycle 3. With this first clock cycle address and the next cycle data sequence, the read and write operations can be pipelined.

The main irradiation mitigation design of the SRAM is TMR. In TMR mode, a one-word data (4 bytes) would be copied separately three times in the same address on different pages in the SRAM, and then the final result is processed by a majority voter component to achieve a single output. In

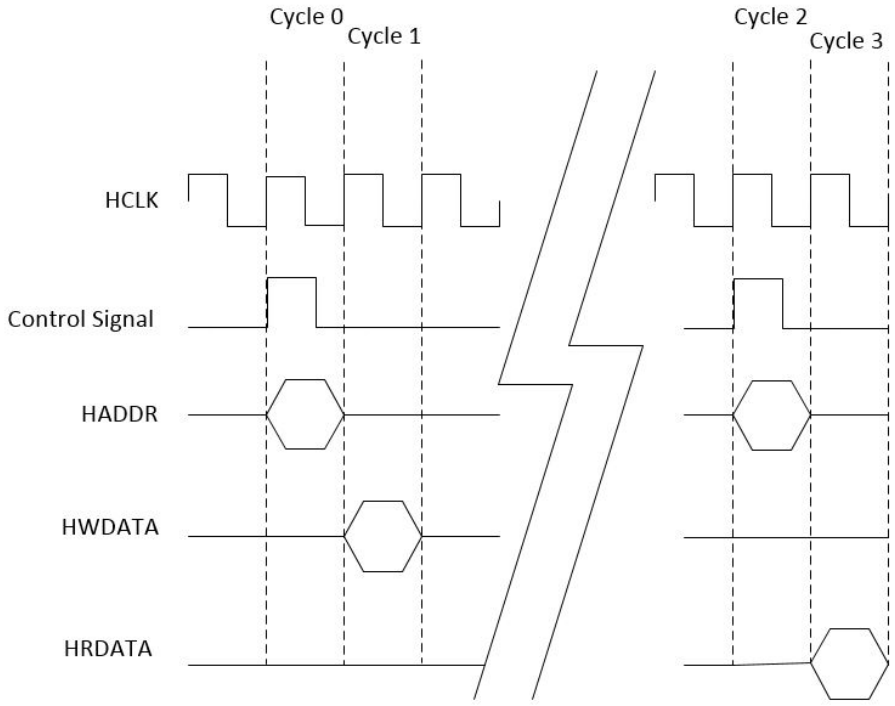



**Figure 3.11:** Operation timing of SRAM

order to operate the SRAM in TMR mode, the CONF_MEN_MODE[2:0] should be configured as 3'b111.

## 3.5 Reference and DICE Flip-flops

Two flip-flop (FF) chains, reference and proposed DICE FFs, were integrated on the test chip. The basic background of the DICE design is introduced in the following section.

### 3.5.1 Dual Interlocked Storage Cell

A Dual Interlocked Storage Cell (DICE) is a basic circuit-level mitigation design proposed by Calin et al [5]. The structure of the DICE is shown as Figure 3.12, which consists of eight transistors or

four pairs of inverters.

If one node has been struck by a particle, the others can help the error node to retain in the correct state and recovery from the soft error. For instance, if node A and C remain at high level (1) while node B and D remain at low level (0), the nodes are stable at this time. In this situation, the states of P0, N1, P2, and N3 are ON. When a particle strikes node B, it can induce a positive voltage pulse. The high logic level of node B would turn off P2 and turn on N0. Node C would remain at its original value because both P2 and N2 are closed. The value of node A depends on the competition between P0 and N0. Whatever the state of node A, the value of node D will keep its initial value (0). After the positive pulse ends, all the nodes can be restored, which means the structure of DICE will be immune to the SEE.

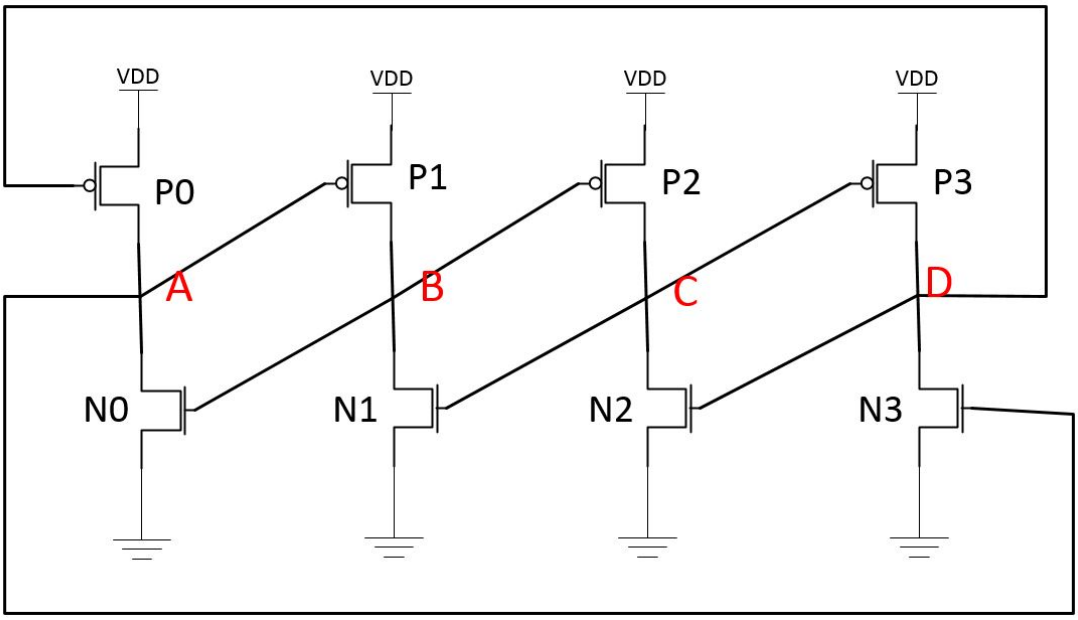



**Figure 3.12:** Structure of DICE [5]

### 3.5.2 Testing Flip-flop Chains

The purpose of these two FFs is to verify independently the effectiveness of the redundancy-based mitigation method (DICE) in the 28nm FDSOI architecture. The reference FF was selected from the standard cell library of the STM. The DICE FF is a custom-designed radiation-hardened FF. The DICE structure is designed as a double-row cell and an assembly of four pairs of inverters with eight transistors.

To verify the radiation performance of these two FF chains, the total of the cell number in each chain is 4256 and 4225 respectively. Both of the chains share a common input port for data and clock, but have different output ports for data. To avoid a hold-time violation, the reversed clock tree system was implemented to drive the two FF chains. In order to reduce the SETs in the clock tree, large clock buffers were applied.

# 4 ARM CORE TESTING SYSTEM DESIGN

## 4.1 Introduction of Test System Components

The purpose of the test system design is to investigate the implementation of different levels of the ARM core in an irradiation environment. This chapter describes the development of the testing system.

As shown in Figure 4.1, this testing system consists of three main parts, including Raspberry Pi, Virtex5 FPGA, and DUT board. Raspberry Pi is the main control component for the entire system and communicates with FPGA through the UART protocol. The configuration information of the DUT chip, such as the testing core number, operating frequency, and test mode, are transmitted from Raspberry Pi to FPGA. When the configuration data arrives at FPGA through the UART, it is analyzed by FPGA and compiled as configuration commands to the DUT. Each command includes 128-bit configuration data, including program data, core information, and clock information, and every 16-bit configuration data is protected with an odd parity bit. These configuration commands are transmitted through a serial configuration interface to control the DUT chip.

### 4.1.1 Introduction of the DUT Board

Figure 4.2 illustrates the front-side of the DUT PCB board, which is used to test the 28nm FDSOI chips with a QFN64 package. The entire board is $17cm \times 15cm$ and is fixed to the stage using four

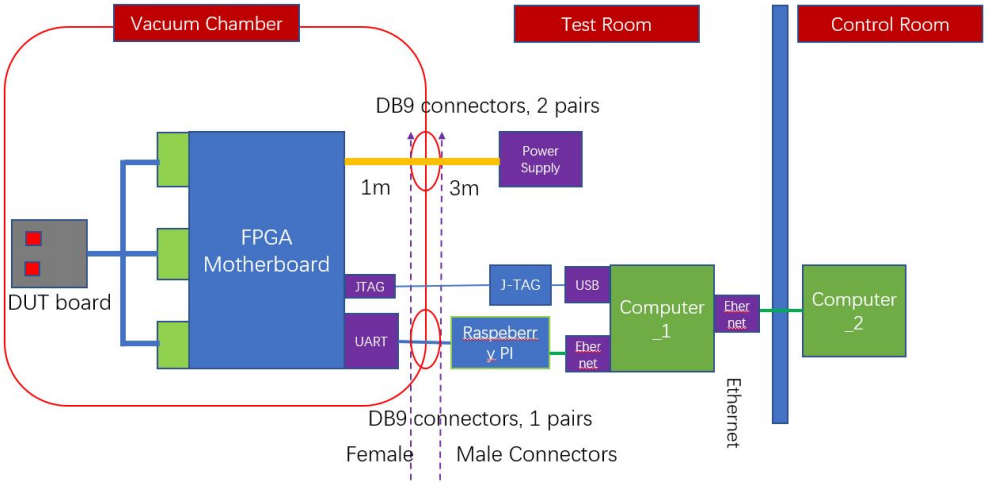



**Figure 4.1:** Architecture of the ARM chip test system for radiation testing

M4 screws. In order to ensure that the laser spot can access the transistors from the substrate, a hole is opened below the back of the test chip through the QFN footprint. The diameter of this hole is $5mm$. The left side of the test board has four banana connectors to supply the power independently. There are two groups of voltages that support the operation of the ARM chip, $1.8V$ power for the I/O pins and $1V$ power for the operating core.

As the Virtex5 FPGA board has three DIMM connectors, four adaption boards are used to connect FPGA and the DUT testing board with a Ribbon cable. It is not necessary for specific impedance adaption, since the communication signals operate at low speed. In the middle of the Ribbon cable, there is a female connector for the probing of any signals for debugging purposes.

## 4.2 ARM Core Test System Design

The DUT is the 28nm FDSOI test chip, including five the different mitigation level design previously mentioned in Chapter 3. This is a collaborative project between the University of Saskatchewan, IROC Technologies, and Cisco Systems. The mitigation methods of combination logic are approx-

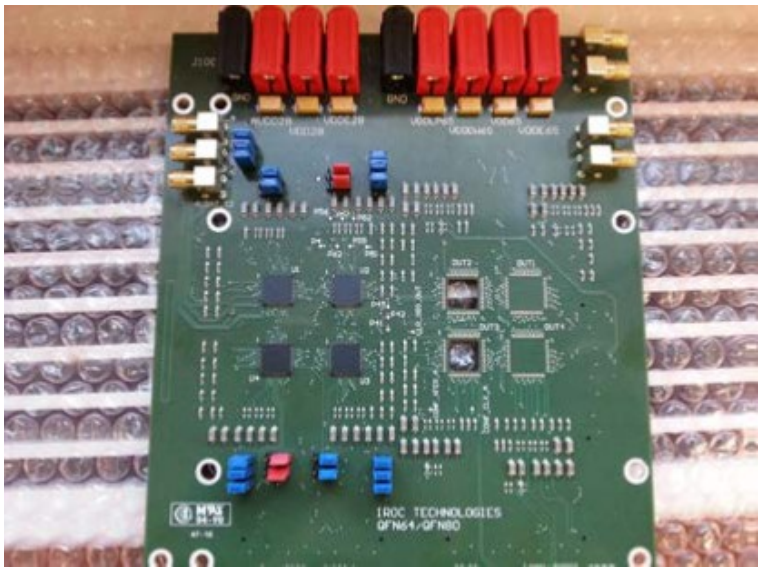



**Figure 4.2:** The Front of the DUT Board

imate logics provided by the University of Madrid, Spain.

The main purpose of the ARM chip test is to study different levels of mitigation techniques on CMOS (Complementary Metal Oxide Semiconductor) technology. ARM chip test should have reliable operations during experiments as it is to be used in different types of irradiation environments, such as laser, heavy-ion, and proton testing. In order to collect enough data to calculate the soft-error cross section, the system needs to run the software testbench continually and verify the result in every iteration. To verify the results of the test, the Cyclic Redunancy Check (CRC) method is used.

### 4.2.1 Cyclic Redundancy Check (CRC) Checksum

In order to collect the data efficiently on the different ARM cores, a checksum operation is performed when the program is complete. When the SRAM component was designed, the CRC circuit was used for calculating the CRC value for its data. In this test system, the CRC checksum is carried out two times in one iteration, the first to write the data into the DUT, and second, to complete

the program run.

CRC is one of the most widely used methods to ensure that data is correct The CRC algorithm as the checksum method was selected for this test system because it can be implemented in a binary storage component directly, and it is accurate. If even a single bit of data is incorrect, an incorrect CRC value would be calculated, which would not match with the ideal reference value. The CRC algorithm considers the binary data to be a coefficient of a polynomial. When this polynomial is shifted and divided by one specific polynomial, there is a reminder polynomial, which is the CRC value, generated.

### 4.2.2 FPGA Program and Communication with Raspberry Pi

The main test system is based on the Virtex5 FPGA. As the name of Virtex5 implies, this is the fifth generation Virtex series of the FPGA developed by Xilinx Inc. The Virtex5 family is designed as a 65nm process technology, and the supply voltage for the internal core is $1V$. The Virtex5 chip is mounted on a test board, as shown in Figure 4.3. The Verilog HDL is the main hardware description language used to describe and build the test system. The objective of this test code is to implement and investigate single event effects, if they occur in a laser, heavy-ion or proton test. In future research, it could be slightly modified for suitable for a specific test.

The structure of the test system is shown in Figure 4.4. There are seven main components in the top level of the test system. The components, configuration drive and status read, are connected with the configuration and status blocks in the ARM chip through the cable, respectively. The architecture for transmitting and receiving data, introduced in Chapter 3, is structured such that FPGA communicates with the DUT through a serial protocol. The frequency of communication is determined by the FPGA, which is generated by the Digital Clock Manager (DCM).

**Figure 4.3:** The Structure of the test system

The instruction decoder section is the main central control component of this system. It maintains the whole system in idle status until it receives a command from Raspberry Pi. The command is a 16-bit binary code, which includes configuration information for the system, such as which core should be tested, which software code should be implemented on that core, on what frequency the core works, and so on. This information can be stored in the command receive center, and then, analyzed and transmitted to the instruction decoder section. The program can operate the system with a Finite State Machine (FSM). The flow of the state machine is illustrated in Figure 4.5. The entire system will remain in the IDLE state. When it receives configuration information from the Raspberry Pi, it enters the CONF (configuration) state. After writing and checking the program code into the SRAM of the ARM chip, the running command transmits from the FPGA to start

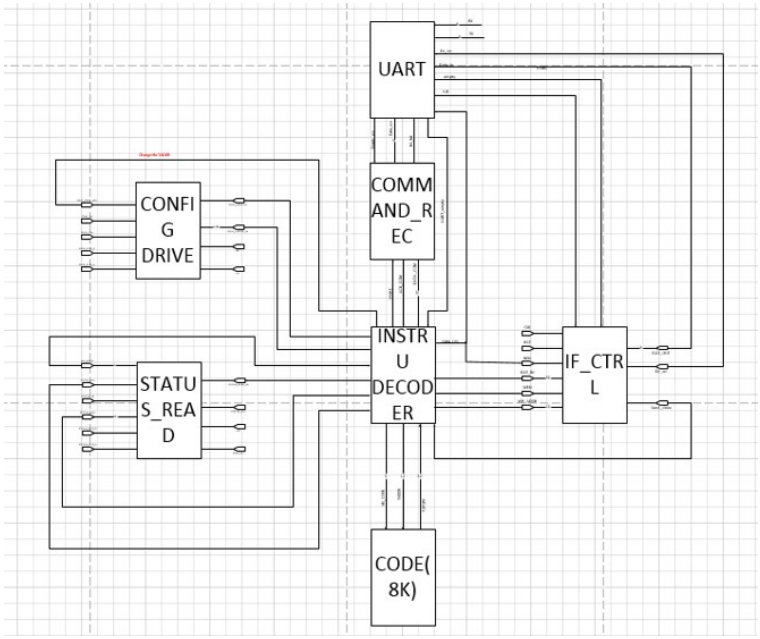



**Figure 4.4:** Structure of FPGA component

the program. There are two inspection steps of the results. First, the FPGA reads out the status information directly to determine whether the program is finished. Second, the FPGA transmits a checksum command to the ARM chip to compare with the ideal checksum result. If there is a difference between the current and the ideal checksum result, it means that there was a SEE during the implementation of the program. If the comparison shows no difference, the FPGA will rerun the test until there is a SEE on the test chip. In the case while the checksum result is different from the golden checksum, the FPGA reads all the information in the SRAM, line by line, and then transmits the entire memory content to the Raspberry Pi for post-analysis. The SRAM of the ARM chip is refreshed with the program and repeats the test in a new round.

The communication protocol between the FPGA and Raspberry Pi is the universal asynchronous receiver-transmitter (UART), one of the most common of the asynchronous communication methods. It just needs only two independently transportation lines, one for receiving and the other for transferring data. Different from other synchronous communication protocols, such as Inter-

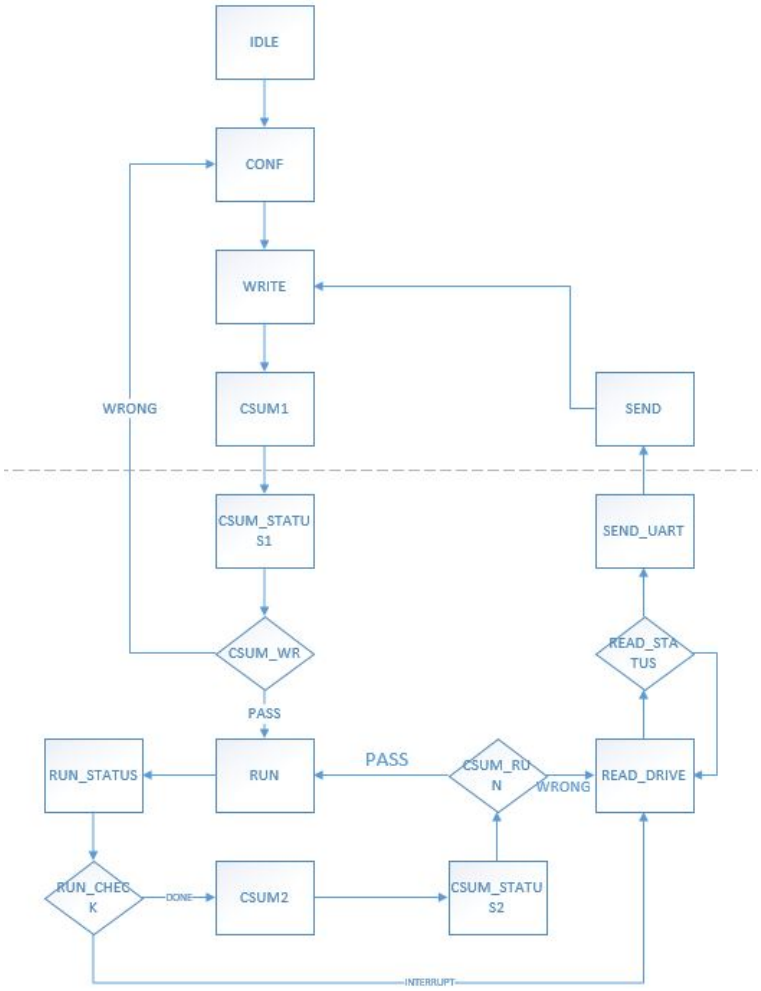



**Figure 4.5:** The flow of the finite state machine

Integrated Circuit (I2C) or Serial Peripheral Interface (SPI), it has no clock signal connection between the two integrated circuits. Each device has a domain clock that can be synchronized using the data itself. The UART protocol cannot transport the data at a higher rate than SPI or I2C, but since the transmission rate is not a critical requirement for the test, the UART protocol was selected as the communication method between the control component (Raspberry Pi) and the FPGA.

There is no synchronous clock signal between the two independent devices (FPGA and Raspberry Pi). The uniform values of the baudrate, used on both sides of transmitting and receiving, is the very important for UART. For the Raspberry Pi, a standard UART protocol can be packeted

and compiled by itself. The user can switch the UART port on and use this function by calling it directly in software. For the FPGA, the UART component must be designed to match with the standard baudrate; otherwise they cannot communicate with each other.

There are several methods to generate the baudrate on the FPGA. One of the most uncomplicated and familiar method is by using a counter directly to calculate and count the value.For example, in this test system, a 50MHz global frequency is provided by the digital clock manager (DCM), and the baudrate for UART communication is 115200. As a result, the signal of the baudrate will flip when the counter has accumulated from 0 to 215. Due to the accuracy of the counter, this method can withstand some errors.

In this system, another method of the baudrate generator will be implemented with higher precision in the phase accumulator. First, the frequency control factor (K) can be calculated by using Equation 4.1. In this test system, the fundamental frequency is the global clock frequency, which is $f_c = 50 \times 10^6 (Hz)$. N depends on the number of counter's digits, which is a 32 in this system. As a result, $K = 85.9 \times f_o$. To configure the baudrate to 115200, the factor (K) should be set to 9,985,680.

$$f_o = \frac{f_c \times K}{2^N} \tag{4.1}$$

Except for the baudrate generator, the main of the UART is a transmitting and receiving interface which operates to transport 8-bit of data. For the transmitting interface, it drives logic high when preparing to start sending data. Then when it is sending data, the 8-bit plus one even party bit are combined and transmitted. For the receiving interface, a higher sampling frequency is used to sample the data.In this way, data sampled at the edge of the signal can be avoided.

### 4.2.3 Embedded Benchmark Software

One of the primary test objectives is to determine a SEE's behavior in combinational logic. In order to observe the effects on the various levels of mitigation designed on ARM cores, different types of benchmark software should be tested on the different cores. Matthew R. Guthaus and his group compared several separate existing embedded testbench suit, and then analyzed a number of areas, including memory behavior and instruction distribution. They concluded that an embedded benchmark can be used for all research [50]. For this test system, the software test cases are based on their benchmarks, but all test cases have been modified to suit our tests. Due to the size of the SRAM, all test cases should not exceed 12KB.

| Embedded Benchmark | Binary Size | Word Size | Slack in Word | Slack in 3K Word |
|---|---|---|---|---|
| Integer square root | 1k | 0.25k | 0.75 | 2.75 |
| Angle conversions | 4k | 1k | 0 | 2 |
| Cubic function | 8k | 2k | -1 | 1 |
| Qsort | 2k | 0.5k | 0.5 | 2.5 |
| Stringsearch | 4k | 1k | 0 | 2 |
| FFT | 7k | 1.75k | -0.75 | 1.25 |
| Bitcount_1 | 2k | 0.5k | 0.5 | 2.5 |
| Bitcount_2 | 1k | 0.25k | 0.75 | 2.75 |

**Table 4.1:** Embedded benchmarks for the test

There are 8 different types of software, as illustrated n table 4.1. These benchmarks are selected to be implemented on the ARM core, and all of them offer different characteristics of the program. There are three basic math algorithm tests, namely are integer square root, angle conversions, and cubic function in the benchmark. The test of integer square root is a simple calculation. Since this algorithm never uses more than half-bit of the squares, there is another exponentiation after it. The test of angle conversion is a function of exchanging between radiant and degree. The examination of the cubic function is a method to solve a cubic polynomial. The qsort test is well known as a quicksort algorithm to sort a vast array of integers from large to small. Sorting the information is the most frequent process used to analyze data in one system. It makes the results more accessible for interpretation, organizes the unsorted data precisely, and reduces the run-time of the program. The string search test searches for specific strings in phrases. It uses the case-insensitive comparison algorithm to recognize the strings and tests manipulation of the text. The Fast Fourier Transform (FFT) is an essential algorithm to obtain frequencies in a given digital signal input. Finally, the purpose of the two bit-count method test is to validate the operational abilities by counting the number of bits in a list.

## 4.3 SRAM Test Design

Although the primary purpose of the experiment is to evaluate the performance of different hardening levels of ARM cores in an irradiation environment, it was found that the radiation effect of its storage component played an important role in the test. At the beginning of the test, the TMR mode of the SRAM was applied in the heavy-ion test to reduce the effects of SEE on it. However, it still had several weaknesses. First, it was assumed that when the program was stored in the SRAM as

TMR mode and implemented on the ARM core, SEEs affected by the SRAM would be ignored. As a result, when an error occurred during the test, it was a soft error in the ARM core. Unfortunately, a comparison of the results of the total of errors and the data from the SRAM indicated that there still were the soft errors caused by the SRAM component. If the fluence and error cross section is calculated in this circumstance, it could less than the actual value.

Furthermore, the TMR mode uses triple the storage of any other mode, which limits the size of the program to 1K words. As mentioned in the last section, there is not enough room for some benchmarks, such as the FFT test or cubic function test. This will be a considerable obstacle in future experiments. The purposes of an SRAM irradiation test is to investigate an SEE on the different modes of the SRAM ingredient without any logic program. The test assists in the study and analysis of the SEU cross section of an SRAM.

In order to investigate the SEU cross section of the storage component, two special test modes, dynamic SRAM test and static SRAM tests, will be executed. As Quinn states in his article, these two type of tests can disclose different characteristics of the component [51]. In the static mode, the SRAM area is full of different patterns. Then the irradiation beam is turned on until the total flux reaches the desired level. The pattern must be one of the three basic data models, namely full ones, full zeroes, or checkerboard. The beam will stop when the static test has been completed.Then all of the data in the SRAM is read back and checked to the original data patterns. Compared with the ideal pattern, the upset cells can be mapped instantly, which aids analysis in the next step. The FPGA program of the test is to transport the specified pattern into the SRAM and then to wait for the DONE command from Raspberry Pi. When the FPGA receives the control signal, it will read back data, line by line, and save it in Raspberry Pi.

In terms of static SRAM testing, basic information about the SEU effect can be achieved

in TMR mode (1K words) and standard mode (3K words). It is necessary to design dynamic SRAM tests to simulate the storage components working in the experimental environment. Dynamic SRAM testing can also be run in two different modes, TMR and flat. During the test, the FPGA will fill the SRAM with the defined data pattern and then check the SRAM, using the CRC checksum function. If the result is different from the ideal consequence, the entire information in the SRAM will be read back and analyzed later. Considering that some of the previous ARM test results are identical to the correct results, it is estimated that a single event may occur in the logic of the CRC check. For this reason, the dynamic SRAM test will be run in a double CRC check, to ensure security and precision.

## 4.4 Setup for Flip-flop Chains on the ARM Chip

There are two FF chains designed in the test chip, the reference FFs and the DICE FFs. Compared with the complexity of a system-on-chip component, the functionality of FFs is more straightforward, that is, the test system for the FF design is also simplistic. Figure 4.6 illustrates the structure of the FFs.

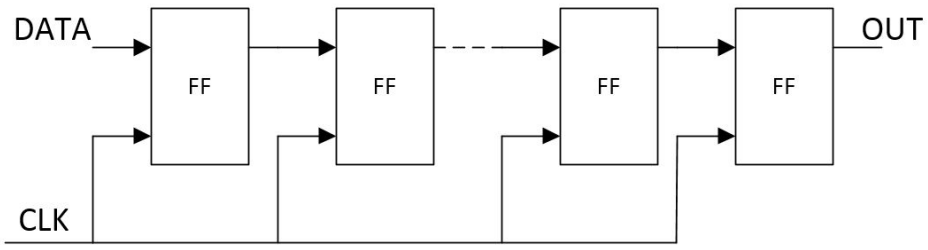



**Figure 4.6:** The structure of the flip-flop chain

On the FPGA side, the system needs to transmit different data patterns. The data will pass

through the chain as the clock is fed to the FFs. On the output side, the testing system should compare the output result from the FF chains continuously. A counter will record the errors when the FPGA receives data that differs from the input data. In this way, the total number of soft error caused by a SEE will be recorded. For the input data pattern of the FFs,one pattern is selected of all ones, all zeroes, or checkerboard to be used during the test.

# 5 CHIP TEST RESULT

## 5.1 The Heavy-Ion Test for the ARM Core

The results presented in this chapter represent the data achieved for the heavy-ion test of the SRAM at the Heavy Ion Single Event Effect Irradiation Facility (HISEEIF) in Beijing, China. The facility and equipment were described in Chapter 2, and a photograph of the whole device setup is provided in Figure 5.1.

The linear energy transfer (LET) is used to describe an ion's energy loss while penetrating silicon, and the unit of LET is $MeV \times cm^2/mg$. As mentioned in Chapter 2, LET can be represented by its energy. The range in silicon represents approximately the distance from the surface of the chip to the point of the ion stopping in the silicon. In the experiment for the SEU of SRAM, the ions whose range in silicon was larger than $30\mu m$ were selected, so that the ions could penetrate the layer of metal and $SiO_2$, reaching the active area of the chip.

### 5.1.1 Experimental Results for the ARM Core

Because of the limitation of the heavy-ion beam time, only two cores could be tested in the time allotted. The reference core and the DICE core, as shown in Figure 5.2, were to perform the heavy-ion test.

The program chosen could search for a specific word or string in a list of sentences. An iter-

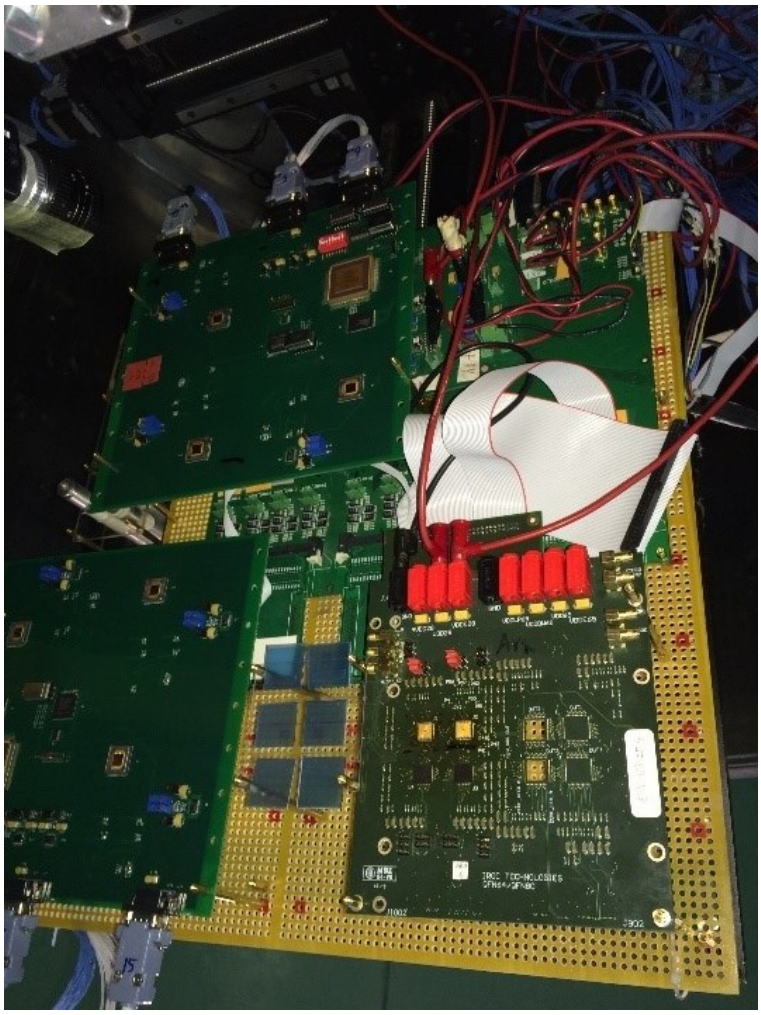


**Figure 5.1:** Picture of ARM test system on the heavy-ion platform

ation of the program is $3.8 \times 10^4$ clock cycles. In order to save time during the experiment, the system will calculate the error number but will not send back the data from the SRAM. In this way, transmission time can be saved and the ARM core affected by the SEU can be observed directly. There are two different types of heavy ion implemented on the test. The first one is to use different LETs of ionization on two cores, and the second is to use one LET with a different work frequency on both cores. A security process was selected to test the ARM core at the very beginning. If 10 soft errors occurred on one core, the test was stopped and accumulated the total fluence was accumulated. After several minutes when the core had recovered, testing of next core began. The

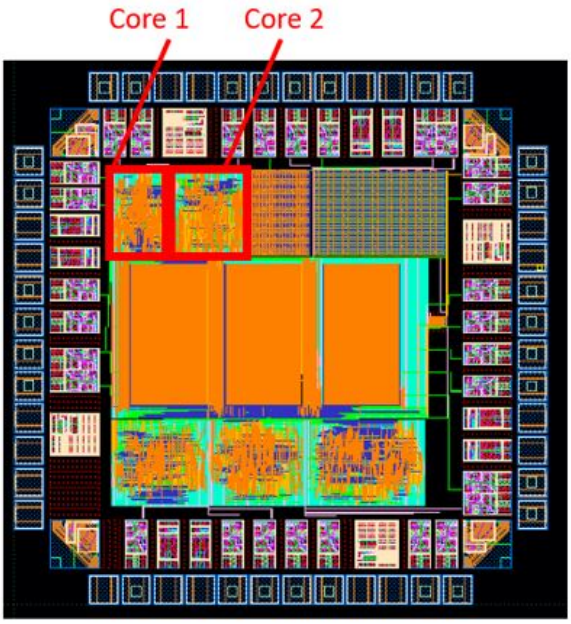



**Figure 5.2:** Diagram of core#1 and core#2

fluence and cross-section of two ARM cores (reference and DICE) with different LETs is shown in Table 5.1.

| LET ($MeV \times cm^2/mg$) | 9.3 | 32.4 | 42.0 |
|---|---|---|---|
| Fluence (core 1) | 1.10E+8 | 1.32E+8 | 4.28E+7 |
| Cross section (core 1) | <9.09E-9 | 7.56E-8 | 2.34E-7 |
| Fluence (core 2) | - | 1.73E+8 | 7.55E+7 |
| Cross section (core 2) | - | 5.77E-8 | 1.32E-7 |

**Table 5.1:** Results of different LET tests

Table 5.2 lists the heavy-ion irradiation results for core 1 of different chips on the DUT board. This test is implemented at different operating frequencies.

After the last iteration of the test, the DUT chip stopped functioning, and at that point, the total fluence was about $2 \times 10^9$. A new DUT board with one new test chip was installed and tested. In this

| Chip and Core | Fluence | Work Freq | SEU count |
|---|---|---|---|
| 1-1 | $4 \times 10^8$ | 608 | 19 |
| 1-1 | $3 \times 10^8$ | 307 | 20 |
| 1-1 | $3 \times 10^8$ | 104 | 22 |
| 2-1 | $3 \times 10^8$ | 104 | 18 |
| 2-1 | $4 \times 10^8$ | 104 | 28 |
| 2-1 | $4 \times 10^8$ | 305 | 29 |
| 2-1 | $4 \times 10^8$ | 305 | 30 |
| 2-1 | $4 \times 10^8$ | 598 | 37 |
| 2-1 | $4 \times 10^8$ | 595 | 41 |

**Table 5.2:** Core 1 test using Cl ion beam

stage of the test, the focus was not just on core 1, core 2 needed to be tested as well for comparison with the reference core. As in the previous test, the chip was implemented at a different frequency. Table 5.3 illustrates the results of the new chip running in core 1 and core 2.

### 5.1.2 Analysis and Discussion

For LET = $9.3 MeV \times cm^2/mg$, there were no errors in the DICE core during the experiment,indicating that the non-hardened core is more sensitive than the DICE one. Based on the formula mentioned in Chapter 2, the cross section can be calculated as

$$\sigma = \frac{errors}{fluence} \tag{5.1}$$

| Chip and Core | Fluence | Work Freq | SEU count |
|---|---|---|---|
| 1-1 | $1 \times 10^8$ | 608 | 6 |
| 1-1 | $1 \times 10^8$ | 320 | 5 |
| 1-1 | $1 \times 10^8$ | 108 | 4 |
| 1-2 | $1 \times 10^8$ | 108 | 5 |
| 1-2 | $1 \times 10^8$ | 320 | 4 |
| 1-2 | $1 \times 10^8$ | 608 | 7 |

**Table 5.3:** New chip test using Cl ion beam

It appears that both cross sections of the DICE core are lower than that of the reference core, which agrees with the expectation before the test. The cross section is plotted in Figure 5.3. However, the cross section of the DICE core decreased 23% and 43% at LET equal to 32.4 and $42.0 MeV \times cm^2/mg$, respectively, which is lower than anticipated [52].

Before the permanent damage to the ARM chip, two groups of data were acquired, but were not enough to calculate an accurate cross section. It is necessary to consider the confidence intervals in the experimental data. The conventional, $2\sigma$ or 95% confidence intervals were used to estimate the range of error bar [51]. Due to the value of the cross section being based on more than 50 events, a normal distribution to approximate the standard deviation was used as shown in the formula:

$$Error - bar = \frac{2 \times \sqrt{events}}{fluence} \tag{5.2}$$

The next phase of the research is focused on the Cl (chlorine) ion, where the value of LET was $15.0\ MeV \times cm^2/mg$. The results of the first tests in the reference core experiment are summarized

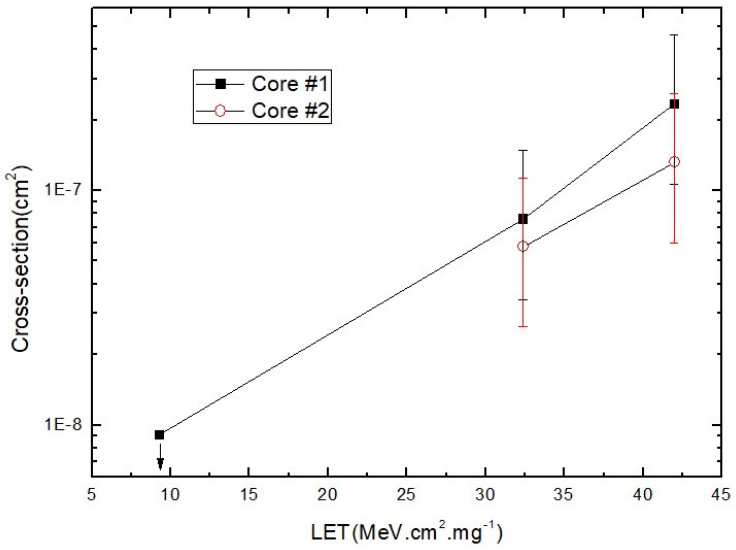



**Figure 5.3:** Previous experiment of core1 and core2

in as Table 5.4. The cross sections were calculated as listed in the table.

| Fluence | Work Freq | SEE count | Cross-section | Error bar |
|---|---|---|---|---|
| $1 \times 10^9$ | 104 | 68 | $6.8 \times 10^{-8}$ | $1.65 \times 10^{-8}$ |
| $1.1 \times 10^9$ | 305 | 79 | $7.18 \times 10^{-8}$ | $1.62 \times 10^{-8}$ |
| $1.2 \times 10^9$ | 600 | 97 | $8.08 \times 10^{-8}$ | $1.64 \times 10^{-8}$ |

**Table 5.4:** Summary of reference core experiment results

The number of soft errors can be converted at the same level of fluence ($1 \times 10^9 ions/cm^2$). Based on this method, when the test was performed at 305 MHz or 600 MHz, it produced 71.8 and 80.8 errors, respectively. This result agrees closely with the research in [20], which reported that the clock frequency was an essential factor when measuring an SEU in a logic circuit. The results also demonstrate that even if the clock frequency is increased to six times the lowest frequency, the number of the soft errors increased by only about 15%. This indicates that the clock frequency's effects are different between the combinational logic and the sequential logic. In this test, the soft

errors induced by an SEU were dominant and not largely affected by the clock frequency. When the clock frequency gradually increased, errors from SETs also increased. Thus, the number of soft errors increased slowly with the increasing clock frequency. We can predict that the SET's soft errors will rise in number with the clock frequency until it is greater than those caused by SEUs, and then SETs become the dominant source of soft errors.

Unfortunately, the test chip stopped functioning after absorbing $6 \times 10^8$ fluence of Cl ions. The plan was to continue testing and acquire more data for analysis. Although this was not possible, the data already acquired could be analyzed and concluded temporarily. Overall, the test system implemented had performed consistently during the heavy-ion testing, and most of the experimental data was reasonable. However, the results of the heavy-ion experiment were slightly different from what was expected before the test. Compared to the normal ARM core, the DICE core, as expected, had fewer errors. Because of based on the independent experimental results of the FF chain, the DICE FFs had much higher radiation resistance than the non-hardened FFs. In the first heavy-ion test, the cross section of the DICE core decreased no more than 50% compared with that of reference core.

There are several possible explanations for the observed results. Firstly, the microprocessor cores shared some common components, such as SRAM and configuration logic. Some errors could be produced by the SEEs in those common components rather than in the independent ARM core. In addition, there are some differences in design for each core. The reference ARM core was implemented with non-hardened flip-flops and combinational logic circuits, along with mitigated clock chains and reset buffers. The DICE core was implemented with hardened flip-flops and clock buffers, but plain logic circuit and reset buffers. Compared with the non-hardened combinational logic circuit in the reference and DICE core, it cannot be assumed that the rest of the designs (except

the DICE structure) are completely the same. As a result, a conservative experimental method, that is, 10 soft errors for each core, was applied in this test, and the error bars also had an unavoidable impact on the experimental results, as shown in Figure 5.3. The overriding range of the error bars prevent us accurate analysis.

## 5.2 The Heavy-Ion Test for SRAM

In the SEE test on the ARM core, the SEU in SRAM could not be ignored simply as a margin of error. The increasing number of radiation-hardened memory components, such as SRAMs or DRAMs, have been used on many modern space systems. As a result, the SEUs in SRAM plays an essential role in the experiment of the complex system. It is illustrated and analyzed at the beginning of this chapter and followed by the result of the ARM core test.

As with all SEE tests, the ARM test system is based on event design. The most significant method in the test is measuring the amount of radiation fluence and calculating the number of errors. Based on the data from these tests, the cross section can be calculated and used to predict the error rate in orbit.

### 5.2.1 Experimental Results For Static SRAM

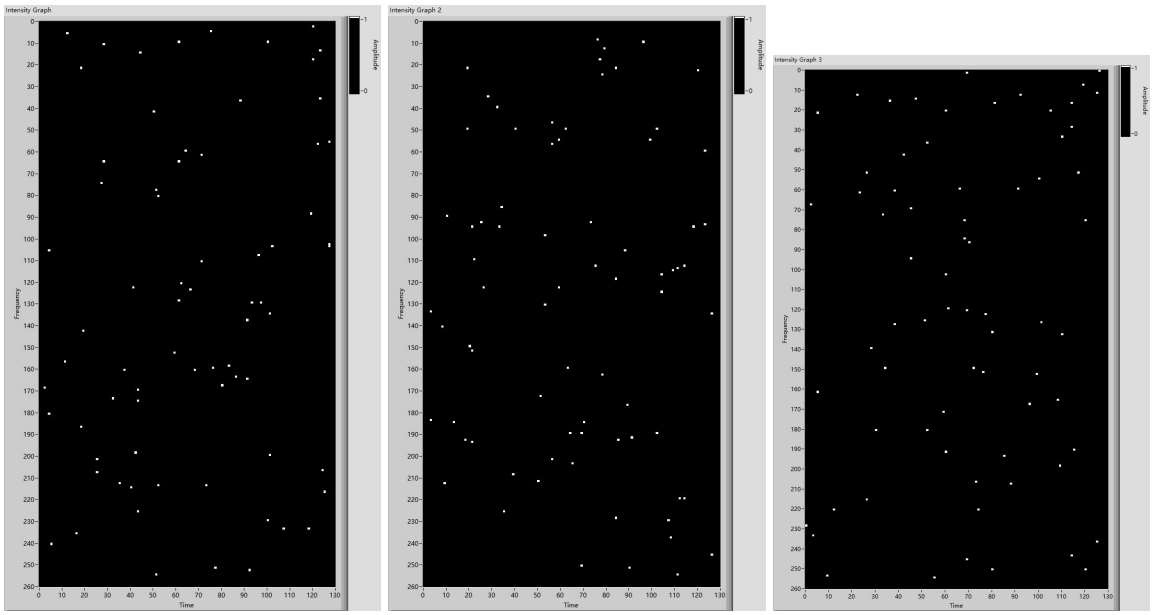
The Cl ion is used as the test ion for the first static SRAM test. The current values of LET and energy are $15MeV \times cm^2/mg$ and $110MeV$, respectively. Due to the limited beam time available, the test was run seven times under the Cl heavy-ion beam, which required ninety minutes. The results of the static SRAM test are shown in Table 5.5.

These results are from the static SRAM experiment in standard mode, which means that the

| Fluence ($ions/cm^2$) | Data pattern | SEU Count | Convert to TMR |
|---|---|---|---|
| $5 \times 10^7$ | all logic one | 973 | 11 |
| $1 \times 10^7$ | all logic one | 216 | 0 |
| $1 \times 10^7$ | all logic zero | 221 | 1 |
| $1 \times 10^7$ | all logic zero | 189 | 0 |
| $1 \times 10^7$ | all logic zero | 215 | 1 |
| $1 \times 10^7$ | all logic zero | 193 | 0 |
| $1 \times 10^7$ | all logic one | 209 | 1 |

**Table 5.5:** The heavy-ion result of static SRAM

three parts of the memory cells were filled with different data patterns (all zeroes or all ones), and they worked independently. Table 5.5 provides the data needed to calculate and analyze the relationship between fluence and SEU, using Cl, which is 201.45 for $1 \times 10^7 ions/cm^{-2}$. After the irradiation beam stopped, all the data in the SRAM was read back, and the register map generated the information shown in Figure 5.4, which shows that when the radiation fluence is $1 \times 10^7$, the total count of SEUs is 216. As described in Chapter 3, these three different banks represent different memory blocks in the SRAM, each block holding 1K words (32K bits). Therefore, the accurate position of the error bit can be easily observed from the diagram. Alter a comparison of all three banks, the data in the same address in each bank was extracted and voted as the output of TMR. Through this simulation of the TMR algorithm, the errors converted to the TMR mode can be calculated and listed, as in the last column of Table 5.5.




**(a)** SRAM bank A **(b)** SRAM bank B **(c)** SRAM bank C

**Figure 5.4:** SRAM register mapping of 216 errors

### 5.2.2 Experimental results for Static TMR SRAM

The TMR algorithm has a simple structure, and is considered widely in space and commerical electronics. Therefore, implementation of testing in the TMR mode is needed. In order to estimate accurately and analyze the number of errors and the cross section, the same type of heavy ions and flux was used to perform the test. Some research shows that the TMR mode is an effective system-level mitigation approach under irradiation conditions [53]. In this experiment, more ion fluence was provided than in the standard mode of an SRAM test for detecting an SEU.

The static test of TMR SRAM was done when the fluence value reached $1 \times 10^8$, which was 10 times higher than in a standard SRAM test. The entire test took almost ninety minutes, and the results are illustrated in the Table 5.6.

Figure 5.5 shows the upside bit in a virtual bank voted by three TMR blocks in the SRAM. The rate of SEUs is significantly lower than the normal SRAM mode, even when the ion fluence

| Fluence $(ions/cm^{-2})$ | Data pattern | SEE Count |
|---|---|---|
| $1 \times 10^8$ | all logic one | 52 |
| $1 \times 10^8$ | all logic one | 49 |
| $1 \times 10^8$ | all logic zero | 34 |
| $1 \times 10^8$ | check board | 53 |

**Table 5.6:** The heavy-ion test results of TMR SRAM

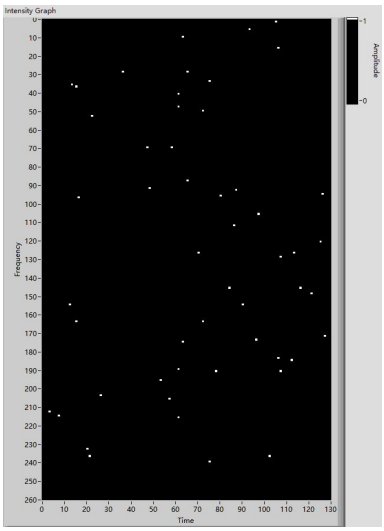
is 10 times higher than the normal mode. It demonstrates and confirms that the TMR mode is an effective and powerful method for protecting device from radiation effects. However, as the fluence increases, more errors are produced in the TMR mode, which may be caused by other factors, such as the total dose.

### 5.2.3 Analysis and Discussion

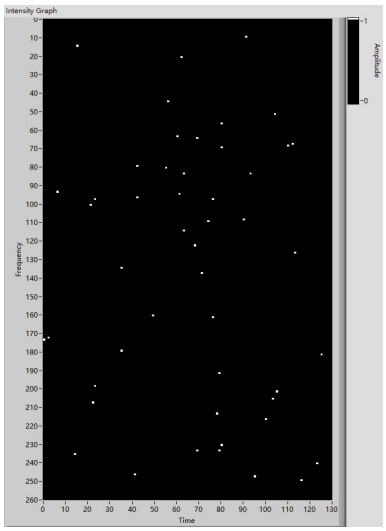
#### 5.2.3.1 The Result of TMR Errors from Statistics

The results of the normal SRAM test can be used to calculate soft errors that occur in TMR mode. A comparison between the estimated soft errors under the TMR SRAM mode and the actual experimental results under the TMR mode can help in investigating this mitigation approach and interpreting the cross section of the SRAM. Based on the normal mode of the SRAM heavy-ion test, the relationship between fluence and SEU counts is shown in Table 5.7.

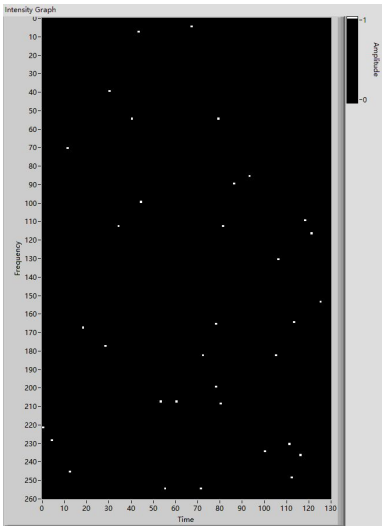
The total number of bits of in the 3K words is $1024 \times 3 \times 32 = 98304$, representing 98304 single-bit cells in the memory segment. The probability of a single cell flipping or double flipping can be calculated with different fluence. In TMR mode, only when two or three bit of copies upside



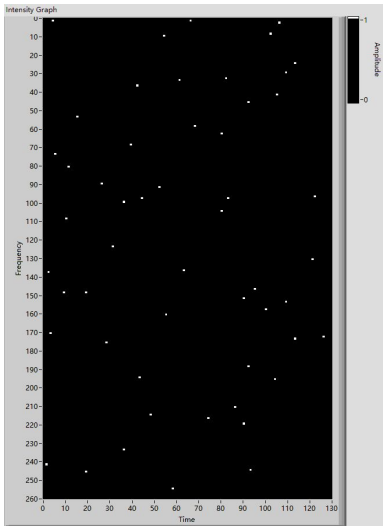

**(a)** 52 error of TMR mode




**(b)** 49 error of TMR mode




**(c)** 34 error of TMR mode




**(d)** 53 error of TMR mode

**Figure 5.5:** TMR SRAM register mapping

simultaneously, the output can be recognized as an error. The probability of twice upside on one bit can be calculated by the formula $P \times P(1\text{-}P) \times C_3^2$, and the probability of an SEU for all three TMR addresses can be estimated by $P \times P \times P$. The entire flipped probabilities summarized these two types of errors, and the chart of TMR error expectation in different fluence is shown in Figure 5.6.

| Fluence ($ions/cm^{-2}$) | SEU | Prob of a single-bit error | Prob of double-bit error |
|---|---|---|---|
| $1 \times 10^8$ | 2000 | 0.02083 | 0.00043 |
| $9 \times 10^7$ | 1800 | 0.01875 | 0.00035 |
| $8 \times 10^7$ | 1600 | 0.01667 | 0.00028 |
| $7 \times 10^7$ | 1400 | 0.01458 | 0.00021 |
| $6 \times 10^7$ | 1200 | 0.0125 | 0.00016 |
| $5 \times 10^7$ | 1000 | 0.01042 | 0.00011 |
| $4 \times 10^7$ | 800 | 0.00833 | 0.00007 |
| $3 \times 10^7$ | 600 | 0.00625 | 0.00004 |
| $2 \times 10^7$ | 400 | 0.00417 | 0.00002 |
| $1 \times 10^7$ | 200 | 0.00208 | 0.000004 |

**Table 5.7:** Relationship between Fluence and SEUs

#### 5.2.3.2 The Actual Result of TMR Errors from the Experiment

The average number of TMR errors for the actual experiment is 47 for a fluence of $1 \times 10^8 ions/cm^{-2}$, as shown in Table 5.6. Unfortunately, due to the heavy-ion beam time limitation and environment requirements, the TMR mode test is implemented for only four iterations, and there was no opportunity for further testing using more or other types of heavy ions or a different flux.

#### 5.2.3.3 Discussion

As shown in Figure 5.6, a comparison between the actual test results and statistical results reveals that the experimental results are basically consistent with the estimated values. Based on this

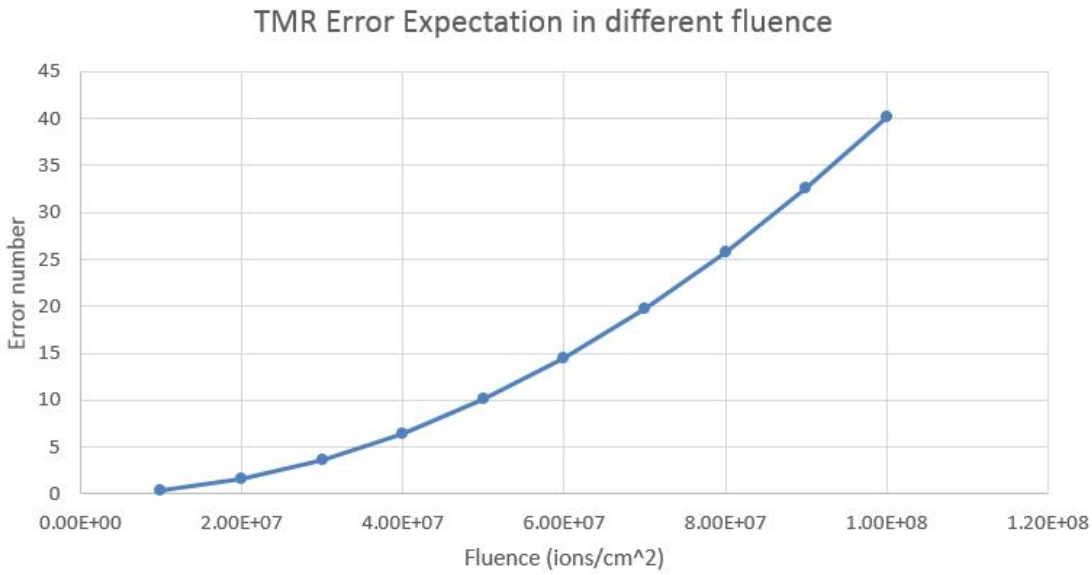



**Figure 5.6:** TMR error expectation in different fluence

comparison, the function of the test system appears to be fundamentally correct. Furthermore, the SEU cross section of the SRAM can be calculated by using the previous experimental data. Table 5.8 shows the values of the SEU cross section in static mode. As indicated in the table, the cross section of the TMR mode is one order of magnitude lower than that of the non-TMR mode, but it is still higher than the cross section of the TMR SRAM mode in the actual experiment, because the SRAM was refreshed and kept in dynamic action during the test. The total SEUs in dynamic TMR mode can be calculated as $5.47 \times 10^{-4}$ in fluence of $1 \times 10^{8} ions/cm^{2}$. The SEU cross section of the dynamic SRAM is estimated at $5.47 \times 10^{-12}$ per device, which is almost negligible in practical applications.

| Fluence ($ions/cm^{-2}$) | mode | SEE counts | cross-section(per bit) |
|---|---|---|---|
| $1.1 \times 10^8$ | non-TMR | 2216 | $2.05 \times 10^{-10}$ |
| $4 \times 10^8$ | TMR | 188 | $1.43 \times 10^{-11}$ |

**Table 5.8:** TMR and non-TMR cross section

## 5.3 The Heavy Ion Test for the Flip-flop Chain

### 5.3.1 Experimental Results for the Flip-flop Chain

As mentioned in Chapter 4, the heavy-ion test for an FF chain is followed by the SRAM test. The data pattern selected was a checkerboard, which was created by the FPGA sending logic high and low periodically as a rectangular wave. When a SET or SEU occurred on one of the FF chains, it caused an upset in the FF. The FPGA found the error by comparing the pattern with the ideal data pattern and reported it to Raspberry Pi. This test was performed at 1MHz clock frequency. There were four types of ions in different LETs, as shown in Table 5.9.

| LET ($MeV \times cm^2/mg$) | Error count | Fluence ($ions/cm^{-2}$) | Cross section (per bit) |
|---|---|---|---|
| 9.3 | 26 | 1.10E+8 | 5.55E-11 |
| 13.4 | 118 | 3.16E+8 | 8.77E-11 |
| 32.4 | 242 | 4.24E+8 | 1.34E-10 |
| 42.0 | 142 | 2.48E+8 | 1.35E-10 |

**Table 5.9:** Result of reference flip-flop chain

The error numbers and the fluence are also shown in Table 5.9. Based on the data acquired from the experiment, the SEU cross section can be calculated.

### 5.3.2 Analysis and Discussion

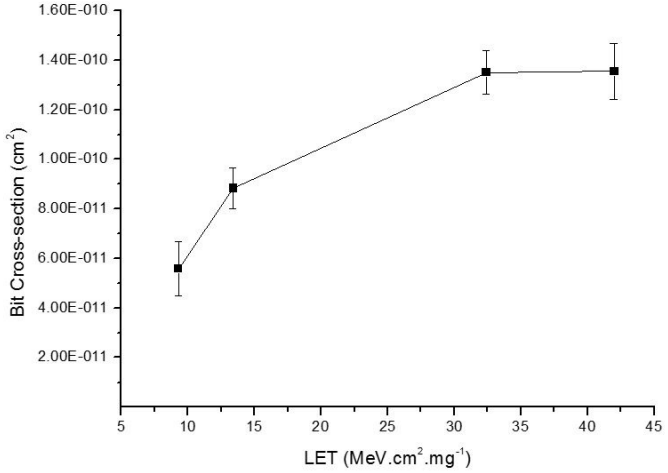



**Figure 5.7:** Flip-flop cross section

Figure 5.7 illustrates the results of the heavy-ion experiment with the checkerboard input. It can be observed that the cross section per bit stage at the same level after an increasing trend with the LET enhanced in reference to the FF chain. In other words, there is no significant change of the cross section between the value of LET from $32.4 MeV \times cm^2/mg$ to $42.0 MeV \times cm^2/mg$. This conclusion is consistent with the assumptions before the experiment. However, it was unexpected that no errors occurred in the DICE chain. Because the test system for the FF chain has the function of self-checking, it was implemented before and after the heavy-ion test to ensure that the chip functioned normally. As a result, this DICE chain had an unexpectedly high SEE tolerance in the radiation environment even with the LET reaching $42 MeV \times cm^2/mg$ [54].

To summarize the FF test, it can be observed that the DICE technology is a powerful and

efficient hardening method to protect FF from radiation effect in the 28nm FDSOI. Moreover, the test was applied on four ARM cores but not the reference core.In the radiation experiment for the ARM test, the SEE on the the DICE flip-flop can be ignored, as there was no soft error when LET was under $42MeV \times cm^2/mg$ in the environment.

# 6 SUMMARY AND FUTURE WORK

## 6.1 Summary

In this thesis, a testing system was developed for investigating single event effects on a custom-developed 28nm FDSOI test chip, which includes a SRAM, reference and DICE flip-flop chains, and different SEE hardening levels of the ARM Cortex-M0 cores. All of these components are integrated into a custom designed chip. Heavy ion experiments were carried out at the Heavy Ion Single Event Effect Irradiation Facility (HISEEIF) in Beijing. The results are presented in this thesis and are summarized as follows:

1. A FPGA-based testing system was successfully developed which included both the hardware and software. The hardware of the testing system is composed with a daughter card on which the test chip is soldered, a FPGA mother board, and a Raspberry Pi module - a tiny single board computer, and a laptop computer. The Ethernet cable was used to connect the laptop computer and the Raspberry Pi, while the communication between the Raspberry Pi and the FPGA board is through a URAT serial cable. The DUT daughter card was directly plugged to the FGPA mother board with a DIM connector. The software package includes the communication and display program for the laptop computer, the control and communication program for the Raspberry Pi computer, and HDL program for the FPGA mother board to configure the daughter card. The system configure the chip to access to the FF chains and

different mitigation types of ARM cores, and read back the experimental data during the test. The developed testing system have successfully carried out the functional test and the heavy ion experiments on the custom-designed test.

2. Measured and evaluated the radiation tolerance of reference and radiation-hardened flip-flops. The observed radiation effects on the reference flip-flop chain agreed with the expected trend of the cross section of FDSOI, and the hardened flip flop chain did not have upset until 42 LET $MeV \times cm^2/mg$. The performance of flip lops proves that the DICE technology of 28nm FDSOI is an effective mitigation method for the flip-flop element.

3. Analyzed the SEE on SRAM designed with 28nm FDSOI technology. Two SRAM testing approaches, static and dynamic were developed for the radiation experiments. However, due to the limits of beam time, only the static test was performed in the experiment. The results showed that SRAMs without TMR presented a relatively low cross section, while the SRM with TMR can effective protect the SRAMs from SEEs. It showed that the soft error rate of the TMR mode is nearly two orders of magnitude smaller than the non-TMR mode.

4. Investigated and measured the soft error rates for different mitigation levels of the ARM Cortex-M0 cores designed with 28nm FDSOI technology. The radiation experiments were mainly concentrated on the reference and DICE cores due to the limited beam time. The results showed that the core with hardened flip flops has lower cross section compared to the core with regular flip flops, which is expected. However, the improvement was only about two times at LET of 42 LET $MeV \times cm^2/mg$. It indicates that more components in a complex system need to be hardened in order to improve the performance of the whole system.

The irradiation results showed that in order to effectively reduce the soft error rate in a complex

digital system, it is not enough just to simply harden the storage cells, more components needs to be considered. This provides a guideline for future investigation for future research in SEE hardening complex digital systems.

## 6.2 Future Work

While this project contributes to the understanding of heavy-ion effects in various types of IC components, there are some further experiments that can be performed in the future. First, the threshold of the DICE flip-flop was not reached in this test, so a higher LET than 42.0 $MeV \times cm^2/mg$ should be tested. Also, instead of the 90 degree angle of the heavy ion beams, other angled heavy ion beams should also be used during future experiments to examine multiple node upset rates in the DICE flip flops. Furthermore, the two other hardened ARM core should be tested in the future heavy ion experiments, and comparison of mitigation performances can be done. Finally, except for the heavy-ion test, there are several other particle tests that need to be implemented, such as proton, alpha and laser tests, to further investigate the performance of the cores in various radiation conditions. To reach a comprehensive conclusion, all the results need to be analyzed and integrated.

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